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SEM ANALYSIS TECHNIQUES FOR LSI MICROCIRCUITS

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SEM ANALYSIS TECHNIQUES FOR LSI MICROCIRCUITS, VOL II

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This report consists of two volumes. The general contents of each is as follows:

Volume I - General Information, 1024 Bit Nichrome Link PROM, 1024 Bit AIM PROM, 256 Bit Static RAM. Volume II - 1024 Bit Static RAM, 4096 Bit Dynamic RAM (SIGATE NMOS), 4096 Bit Dynamic RAM (I^2L Bipolar), Summary.

RADC-TR-80-250, Vol II (of two) has been reviewed and is approved for publication.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Scanning Electron Microscope (SEM) Applications were developed and demonstrated for determining circuit configuration and organization. These applications employ voltage contrast and Electron Bean Induced Current (EBIC) techniques. Procedures were developed utilizing these applications to evaluate semiconductor memory circuits.

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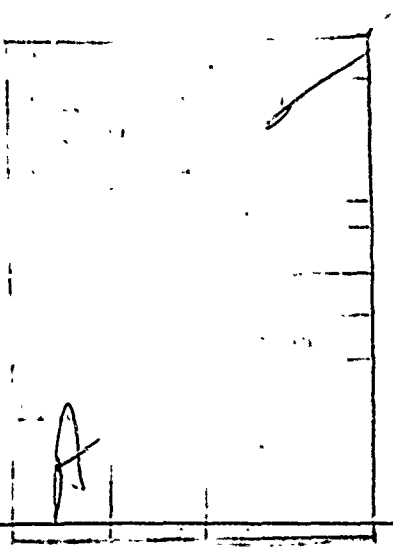
These procedures provide practical methods for developing die maps, electrical circuit schematics, logic diagrams, device block diagrams and memory array bit maps. The SEM data are used in conjunction with light microscopy data to provide significant improvements in device characterization.

The memory circuits evaluated included PROMS, static and dynamic RAMS that utilized bipolar and NMOS process technologies. A total of seven circuit types were evaluated. Voltage contrast provides visual display of multiple circuit states in a single photograph. This technique is called functional mapping. It provides quick location of circuit components related to a specific functional circuit and accurate portrayal of circuit operation. Also a circuit was developed which provides high frequency functional mapping through beam blanking. EBIC evaluation is limited to bipolar and metal gate MOS because silicon gate MOS experiences severe radiation damage. EBIC identifies the diffusion locations and polarity for a major portion of a memory circuit. It is limited by parallel current paths internal to the device circuit. EBIC was found to be invaluable for schematic development of I^2L circuits.

Intentionally generated failures were utilized to demonstrate the feasibility of utilizing SEM applications for isolating circuit failures. The SEM was shown to be a valuable tool for failure isolation.

SEM operating guidelines recommend parameters and techniques for optimum instrument performance and minimal device degradation during evaluation. Limitations experienced for these applications are described. These applications utilize a conventional SEM instrument.



4.5 1024 BIT STATIC RAM (SiGATE NMOS)

Silicon Gate NMOS Static RAM

This device is a 1024 x 1 bit silicon gate NMOS static RAM. The circuit evaluated provides one chip enable and a three state output circuit. The device is packaged in a 16 pin ceramic dip with a ceramic lid.

Electrical Characterization

Eight good devices of this part type were used for this program. In addition there were several reject samples which were primarily utilized for evaluating glass removal techniques.

The eight devices were serialized and electrically tested in accordance with the suppliers data sheet. The DC parameters were measured, recorded and listed according to serial number in Table 5-I. All parameters were verified to meet the vendor specifications.

These devices were then functionally tested as follows. Highs were written into all locations on the device and then read out. The addresses and outputs were applied to a Hewlett-Packard Model 1610A Logic Analyzer with the trigger set in the don't care position for the addresses and in the low position for the output connection. If the output goes low the Logic Analyzer will trigger and the address which is in error will be displayed on the CRT. If no trigger is received then the CRT remains blank and the device is functioning properly. Lows are then written into the devices and checked in a similar manner to that described above. 1, 0 patterns are then written into the device and checked. Ten separate patterns are written in starting with alternating 0, 1, 0,1 . . ., up to 512 0's and 512 1's. This allows each of the ten addresses to be completely checked functionally. This test was run at appproximately 100 kHz (LSB) and found the eight good devices to be fully functional. The functional test procedure is covered more thoroughly in the general text.

Package Delid and Glass Passivation Removal

This device is a 16 pin dual-in-line ceramic package. The package lid was removed by grinding using a diamond impregnated wheel until the lid was thin enough that the cavity could be entered using a sharp probe. This opened the devices with very little contamination being introduced and no damage to the die or interconnect wires.

The glass passivation removal process was tried on the functional rejects first. A number of different procedures were experimented with which resulted in the devices becoming totally non-functional. The supply current would increase dramatically and data could not be written into the memory.

The etchant which was used for obtaining a functional device for the voltage contrast work was 8 parts NH_4 F (40%) to 1 part HF (48%). This etch took approximately 3 minutes to remove enough glass for voltage contrast. These

devices were extremely sensitive to damage from the electron beam and one concern was that if too much of the glass was removed the susceptibility would be increased to the point that voltage contrast could not be performed. Using the above etching time, voltage contrast evaluation could be performed and the device continued to work properly.

Serial number 2 was then stripped and a photograph of the complete die was taken (ref Photo 5-1). The layout of this die has part of the decode circuits located through the middle of the die.

Circuit Characterization

Serial number 2 was placed in a SEM test socket which provides electrical connection between the device and an external connector on the SEM specimen stage. Complete functional testing could then be performed on the device while viewing its operation using voltage contrast on the SEM.

The acceleration voltage used for the voltage contrast examination was 1.5 KV. An acceleration voltage of 5 KV was found to cause permanent device damage, therefore, the examination was performed at a point well below this but at a high enough level to obtain good resolution.

The device was operated at low frequencies; 1 to 20 Hz, while observing the different sections and gaining a familiarization with the device layout. The individual sections were then examined and photographed. The first circuit to be described is the row address buffer. The input discussed is address A2, pin 5. The voltage contrast image is shown in Photo 5-2. The bright areas are at ground potential while the darkest areas are at Vcc. The large bright area in the top left of the photograph is the ground buss metallization. The alternating bright and dark areas in the lower part of the photograph are due to a low frequency (0.6 Hz) square wave being applied to the A2 address. The section of the circuit associated with this input can then be recognized by the similarity of the bright and dark areas. In the top right hand area of the photograph the A2 and A2-not addresses are visible and it is apparent that they are of opposite phase. The light microscope image is shown in Photo 5-3. A comparison of these two photos dramatically illustrates the amount of data present in the voltage contrast photo. The schematic of this circuit is shown in Figure 5-1 and the logic diagram is shown in Figure 5-2. These are developed by using both the light microscope image and the voltage contrast image. The signal is followed through the circuit and the transistors are identified. If a question arises as to the operation of the circuit the part is reexamined and the layout verified. This integrated circuit uses n-channel silicon gate technology. There are two types of NMOS transistors; a depletion mode device such as transistor Q2 and an enhancement mode device such as transistor Q1. The input has a diffused resistor R1 to provide input protection. This is an n-diffusion and is common to the drain of transistor Q1. Transistor Q1 will conduct if A2 is taken negative past the threshold point, thus providing reverse bias protection. When A2 goes high, transistor Q3 is turned on thus pulling the drain of Q3 low This point is connected to the gate of the depletion mode transistor Q2 so when it goes low it increases the re-

sistance of Q2 and therefore, minimizes the current flow and power dissipation. This type of inverter stage is used three places in this circuit followed by an ouput stage for both the A2 and A2-not signals. The output stages are identical except for being opposite in phase. Ion implantation is used during the manufacturing process to adjust the threshold voltage of the devices so that the enhancement mode transistors will function properly with a 5 volt gate voltage applied. The depletion mode devices are also created by heavily doping with ion implantation. The depletion mode devices are always connected like transistor Q2 with the source shorted to the gate.

These two signals from each of the inputs A0 - A4, then go to the Row Decode section of the device. The voltage contrast image of this area is shown in Photo 5-4 and the light microscope image is shown in Photo 5-5. The voltage contrast photo was taken with address A3 cycling at 0.6 Hz, A1 and A2 high and A0 and A4 low. The address signals coming in are labeled as well as the transistors associated with one row. A3 and A3-not are cycling between a high and low state while the remaining signals are being held constant. The schematic for this section is shown in Figure 5-3 and the logic diagram is shown in Figure 5-4. The five input signals are in parallel so that if any input is high the output will be low (disabled). The source region for Q1, Q3, and Q4 are common for this row and Q2 and Q5 source regions are a common diffusion. These two areas are both connected to the ground metallization stripe. These five transistors have a common drain region which goes to the pull up transistor Q6 and to the memory.

To select a particular word in the memory a column must also be addressed. The column address buffer will be described next. A6, pin 1 is shown in the light microscope image in Photo 5-6 and in the voltage contrast image in Photo 5-7. The voltage contrast photo was taken with A6 cycling at 0.6 Hz. Again the portion of the circuit associated with the A6 pin can be easily identified by the striped pattern on the voltage contrast photograph. The circuit schematic is shown in Figure 5-5 and the logic diagram is shown in Figure 5-6. These are identical to the row address buffer and will not be discussed here. The two signals produced by this circuit go into the column decoder.

The signals from inputs A5 - A9 go into the column decode which is shown in the light microscope image, Photo 5-8, and in the voltage contrast image, Photo 5-9. The voltage contrast photo was taken with A6 cycling at 0.6 Hz, A7 high and, A5, A8 and A9 low. The incoming signals are labeled as well as the transistors associated with one column. Functionally this section is the same as the row decode section as shown in the logic diagram in Figure 5-7. However, instead of a single pull-up transistor there are five separate transistors which are connected to the complementary inputs of the five parallel transistors (Figure 5-8). If any of the inputs to the parallel transistors is high the output is low (disabled). If all of the inputs are low the output will be high. The output goes into the sense amplifier circuitry. The circuits which interface with this sense amplifier will be described next followed by the description of the sense amplifier circuit.

The chip enable circuit is shown in the light microscope image, Photo 5-10, and the voltage contrast image, Photo 5-11. The voltage contrast photo was taken with CE cycling at 0.6 Hz. The logic diagram is shown in Figure 5-9 and the schematic is shown in Figure 5-10. This circuit has the same type of input protect circuitry as previously described followed by two inverter circuits. The output, which is in phase with the input, goes to the input data control circuit and to the output circuit.

The read/write buffer is identical to the chip enable circuit and is shown in Photos 5-12 and 5-13 and in Figures 5-11 and 5-12. The voltage contrast Photo 5-13 was taken with R/W cycling at 0.6 Hz. The output from this also goes to the input data control circuit.

The data in buffer has one more inverter stage than the two previous circuits; however, other than that it is identical. It is shown in Photos 5-14 and 5-15 and in Figures 5-13 and 5-14. The 0.6 Hz square wave signal was applied to the data input. There are two outputs generated, data in and data in-not, and these also go to the input data control.

The input data control receives the chip enable-not signal, the read/write signal, the data in signal and the data in-not signal. This area is shown in the light microscope image in Photo 5-16 and in the SEM voltage contrast image in Photo 5-17. In the voltage contrast image the read/write line is changing between a high and low state at 0.6 Hz, data in-not is high (going to transistor Q1), data in is low (going to transistor Q8), and chip enable-not is low. The schematic for this section is shown in Figure 5-15 and the logic diagram is shown in Figure 5-16. As can be seen in the schematic there are two identical circuits which supply signals to the sense amplifier, these are marked number 1 and number 2. A high output from this section going to the sense amplifier is a disabled condition. To obtain a low condition on the output, chip enable-not, and read/write must be low. A low output will occur on the number 1 output if data in-not is low and a low output will occur on the number 2 output if data in is low. These two inputs are complementary so only one low condition can occur. If chip enable-not or read/write is high the two outputs from this circuit will be high (disabled).

In addition to these two signals, two signals from the memory go into the sense amplifier. The memory circuit will be covered next followed by the sense amplifier circuit.

A memory cell is shown in the light microscope image in Photo 5-18 and in the SEM voltage contrast image in Photo 5-19. The cell consists of six transistors, with Q1 and Q6 being the interface transistors to the sense amplifier. The gates of these transistors are tied to a common polysilicon conductor which is connected to the row decode. These transistors are then connected to the sense amplifier by the two metallization stripes. In the voltage contrast photo these two lines are alternating out of phase between a high and low state. This photo was taken with CE, R/W, A6, and A7 low, A0-A5, A8 and A9 high and data in cycling at 0.6 Hz. The memory is being written into, and the cell is therefore changing states. The circuit sche-

matic is shown in Figure 5-17 and the logic diagram is shown ir Figure 5-18. The memory cell functions like a flip-flop circuit with the only modification being that the input and output to the flip-flop are physically the same line. To understand how this can work the sense amplifier must be examined.

There is a sense amplifier for each co'umn of data. The inputs to this circuit come from the data input control circuitry and the memory cell. The output of the circuit goes to the output buffer. This area is shown in the light microscope image, Photo 5-20 and in the voltage contrast image, Photo 5-21. In the voltage contrast image the two end sense amplifiers are being addressed alternately. This photo was taken with inputs A5-A8 low and A9 cycling at 0.6 Hz. When addressed, the column decode line which goes to the gates of transistors Q1, Q2, Q9 and Q11 appears dark. The schematic of this area is shown in Figure 5-19 and the logic diagram is shown in Figure 5-20. With the chip enabled and in the write mode the data from the input data control will be high on either transistor Q1 and Q2 and low on the other transistor. These transistors will be turned on by the column decode signal and the data will be transferred to the memory. At the memory the state will be set by the low input turning off the transistor to which it goes, either Q3 or Q5. When that transistor turns off its drain goes high and turns on the other transistor in that pair. The memory cell will stay in that state until a low occurs on the gate of the transistor which was previously turned on.

In the read mode the inputs from the input data control to transistors Q1 and Q2 in the sense amplifier will both be high. In this mode they will not change the state of the memory cell. The transistor in the memory cell which is turned on will sink additional current but the drain will not go high enough to switch the cell. One of the two memory data inputs to the sense amplifier is low and the second one is high. The one which is low transfers through either Q5 or Q6 to the output transistor Q12 or Q13. This output transistor is turned off and the drain appears to be a high impedance. The other output transistor will be turned on and will be low due to transistor Q11 being turned on. These two lines, one appearing as a high impedance and the second as a low impedance go to the output buffer.

The light microscope image of the output buffer section is shown in Photo 5-22 and the voltage contrast image is shown in Photo 5-23. The voltage contrast photo was taken with A0-A3 high, A4-A8 low, A9 cycling at 0.6 Hz with alternating highs and lows written in memory. The inputs to this section are the chip enable-not line and the two signals from the sense amplifier. The circuit schematic is shown in Figure 5-21 and the logic diagram is shown in Figure 5-22. The Data line is on the left in the schematic and the Data-not line is on the right. With CE-not low and a high on the Data line a high will appear at the output. If CE-not goes high, transistors Q25 and Q26 are turned off and the output appears to be a high impedance.

The chip organization is shown in Photo 5-24. A block diagram is shown in Figure 5-23. The die dimensions are 130 mils by 130 mils and the die has

aluminum metallization and aluminum ultrasonic bonds. A bit map was also generated and is shown in Figure 5-24.

Electron Beam Induced Current examination of this device was attempted with little success. Serial number 4 was decapped and tested to be fully functional. The I_{CC} at this time measured 25 mA. Examination in the SEM was begun at 2 KV acceleration voltage and slowly increased. At 5 KV EBIC was just becoming visible. At 8 KV the device had become too leaky to perform EBIC examination. The device was then electrically tested and found to have no functional response and I_{CC} of 100 mA. The part was baked at 250°C for 10 minutes with a nitrogen purge. No change in its performance was noted. It was then baked for a total of 30 minutes at 300°C and retested. It was still nonfunctional and had a high Icc. Examination on the SEM at 1.5 KV using voltage contrast found only one row address functioning on the device.

EBIC was then attempted on a second device, S/N 6. The results were similar with permanent damage resulting at 5.5 KV.

As a result of this examination it was determined that EBIC was not a viable technique for working with n-channel MOS silicon gate devices.

Failure Analysis

A failure was produced on serial number 16 by electron beam exposure in a small area on row address A2 for approximately 10 seconds in the SEM at an accelerating voltage of 6 KV. This address became non-functional.

The part was then given to a second person for failure analysis. Functional testing found that zeros, ones, and alternating zeros and ones could be loaded into all addresses except A2. The problem was therefore, related to address A2 or to the decode section.

The device was placed in the SEM with an accelerating voltage of 1.5 KV and the address buffer was seen to be non-functional. The signal propogated into the gate of Q5 and then stopped (Photo 5-25 and 5-26). Address A2 was being cycled at 0.6 Hz. Reference Figure 5-1 for the schematic of this area. This condition could occur if Q4 was open or Q5 was leaky. There was no evidence of an open condition on Q4 so it was concluded that Q5 was leaky. Comparison of Photo 5-2 and 5-26 shows the difference between a working address buffer and this failed unit. NOTE: Transistor Q5 was the device exposed to the 6 KV electron beam to produce this failure.

The output section on a second device, S/N 12, was exposed to a 6 KV electron beam for 10 seconds which resulted in the output staying low. Reference Figure 5-21 for the circuit schematic.

The analysis proceeded as follows. Functional testing of the part was unsuccessful. On power up all addresses showed data output was low. Writing data into the memory was also unsuccessful. A check of the output terminal

with a scope showed a zero to one volt swing. This signal could be disabled by switching the chip enable high. This indicated that the problem was located in the data output stage. This was further verified by checking the zero to one volt output while writing into the device. The part responded to the input.

The output circuit was then examined by voltage contrast (Photo 5-27). This photo can be compared with normal circuit operation in Photo 5-23. This photo was taken with all addresses active (LSB = 0.6 Hz) and alternating highs and lows written in memory. It was noted that the voltage contrast was not as dark on the Q23 drain as compared with the Q24 drain (Photo 5-28). The gate voltage on Q17 exhibited a normal voltage swing. It was therefore concluded that either Q15 was not turning on completely, or that Q17 or Q23 were not turning off completely. One of the latter two was the most likely. Closer examination of Photo 5-28 revealed the positive swing of the Q19 source was darker (more positive) than the drain. This indicates the leakage path is on the drain side or Q23 side of Q19. NOTE: Transistor Q23 was the device exposed to the 6 KV electron beam to produce this failure.

TABLE 5-I DC PARAMETERS

SUPPLY CURRENT ICC mA		INPUT LOAD CURRENT I_{LI} µA		OUTPUT LEAKAGE CURRENT Vout=VoH I_{LOH} µA		OUTPUT LEAKAGE CURRENT Vout=0.4V I_{LOL} µA			S/N
36.0mA		<100nA		0.1 µA		-0.5 µA			1
26.3		<100nA		0.1		-0.5			2
28.7		<100nA		0.1		-0.5			3
26.0		<100nA		0.1		-0.5			4
23.7		<100nA		0.1		-0.5			5
37.5		<100nA		0.1		-0.5			6
35.7		<100nA		0.1		-0.5			7
39.1		<100nA		0.1		-0.5			8
									SPEC
55/—		10/—		5/—		-10/—			MAX/MIN

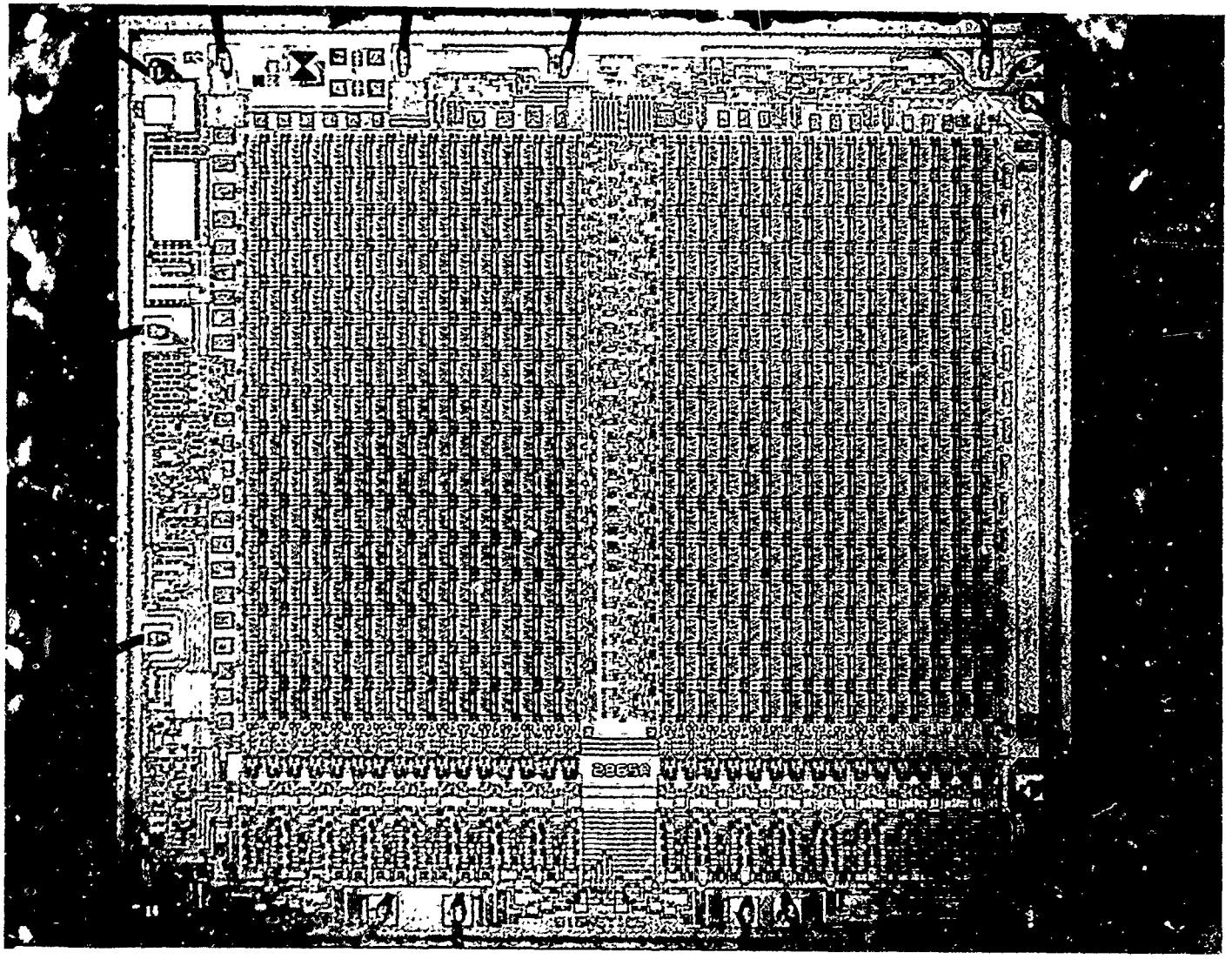


Photo 5-1 Light Photograph of the Complete Die Showing the Pin Locations. Mag. - 45X

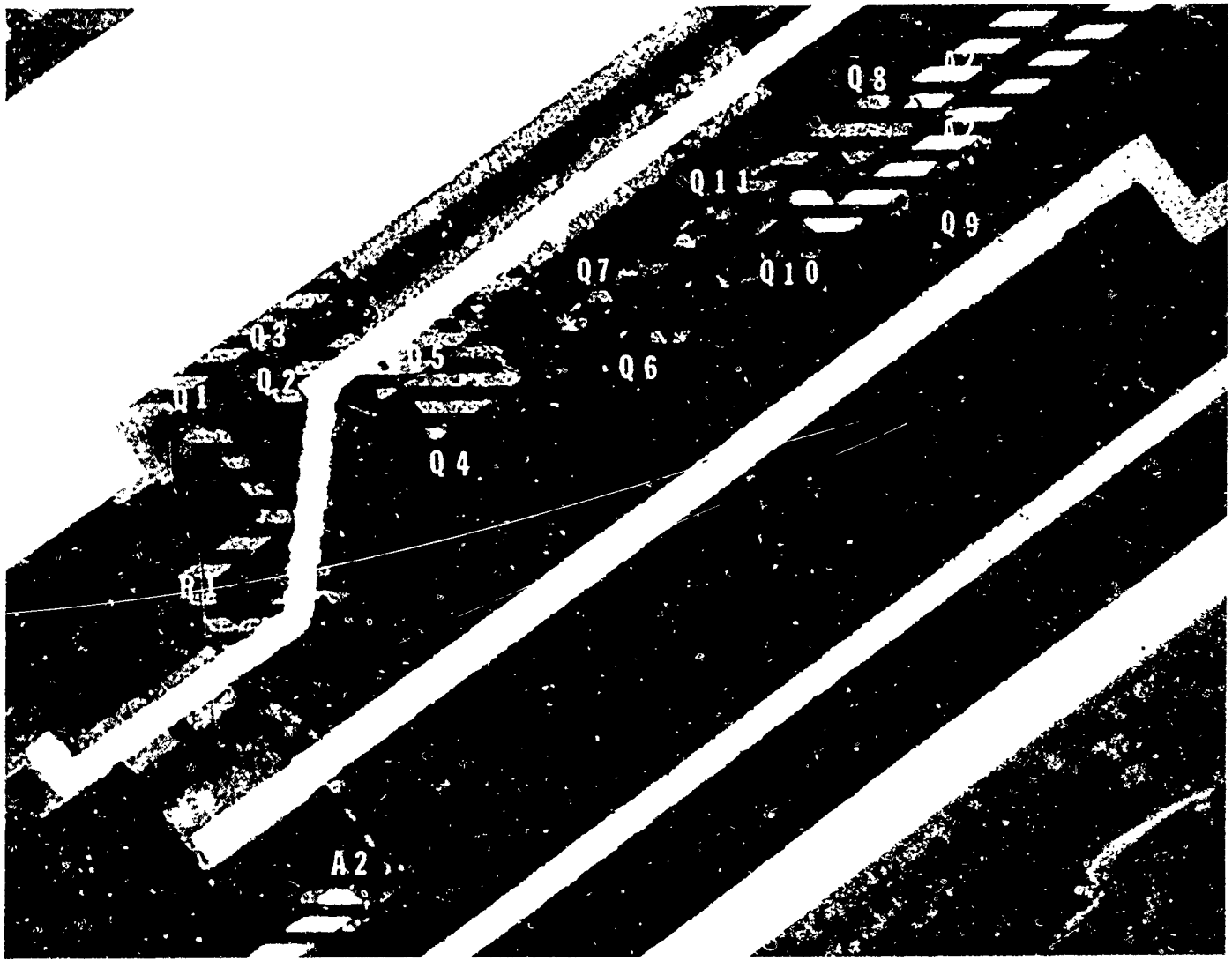


Photo 5-2 Voltage Contrast Micrograph of the A2 Row Address Buffer. 1.5 KV, Mag. - 525X

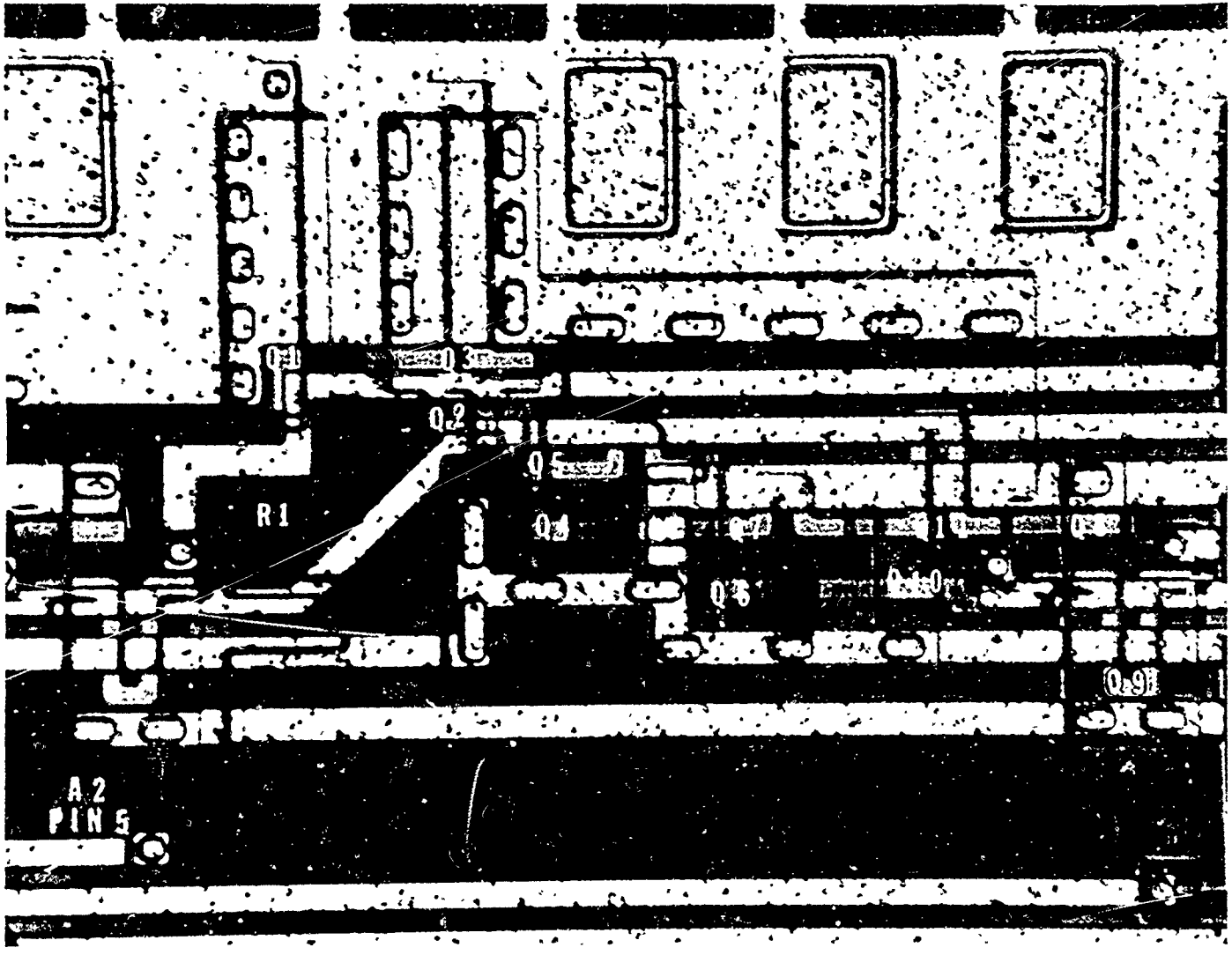


Photo 5-3 Light Photograph of the A2 Row Address Buffer. Mag. - 460X

Photo 5-4 Voltage Contrast Micrograph of a Row Decode Gate Including Identification of the Row Address Busses. 1.5 KV, Mag. - 850X

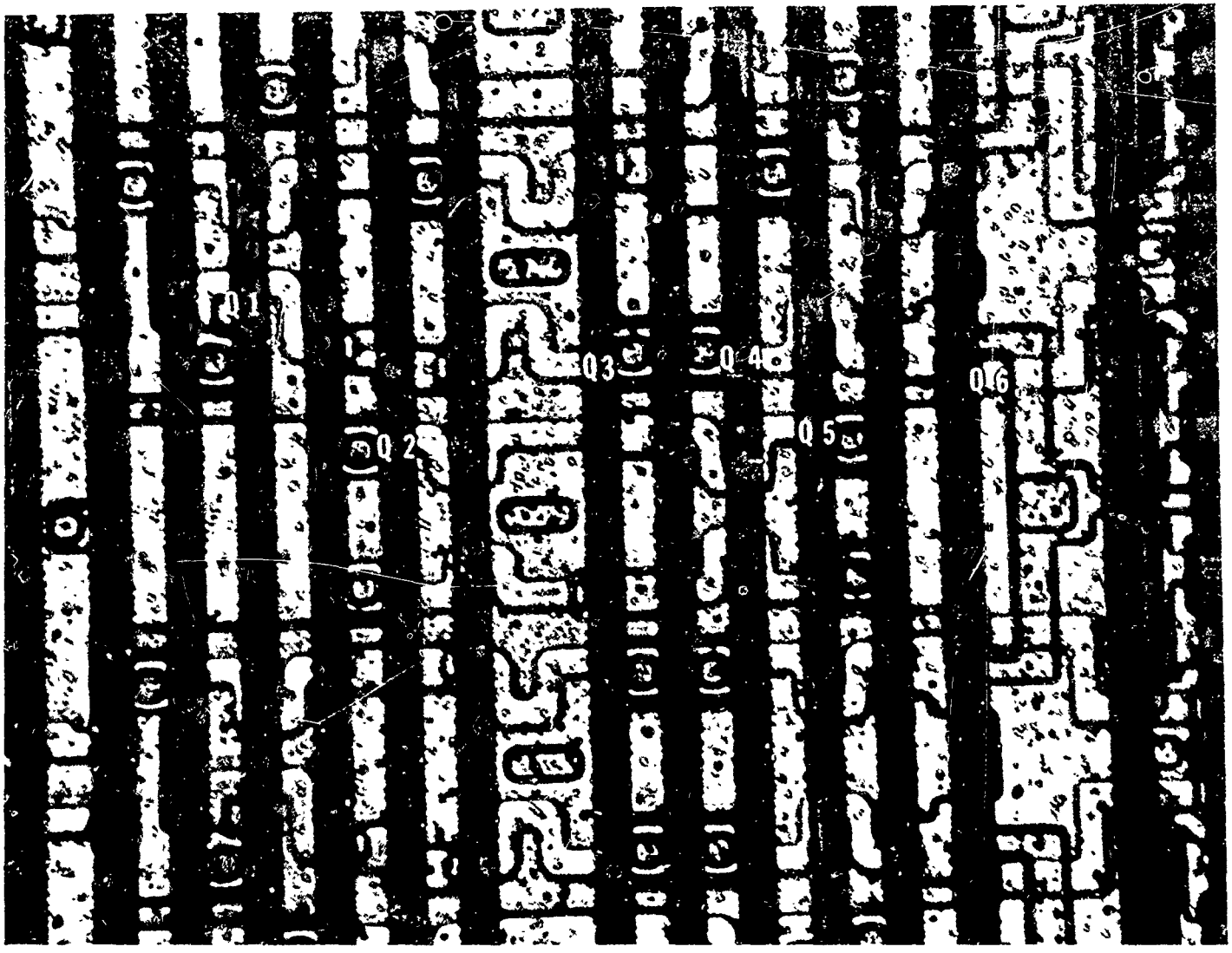


Photo 5-5 Light Photograph of a Row Decode Gate. Mag. - 580X

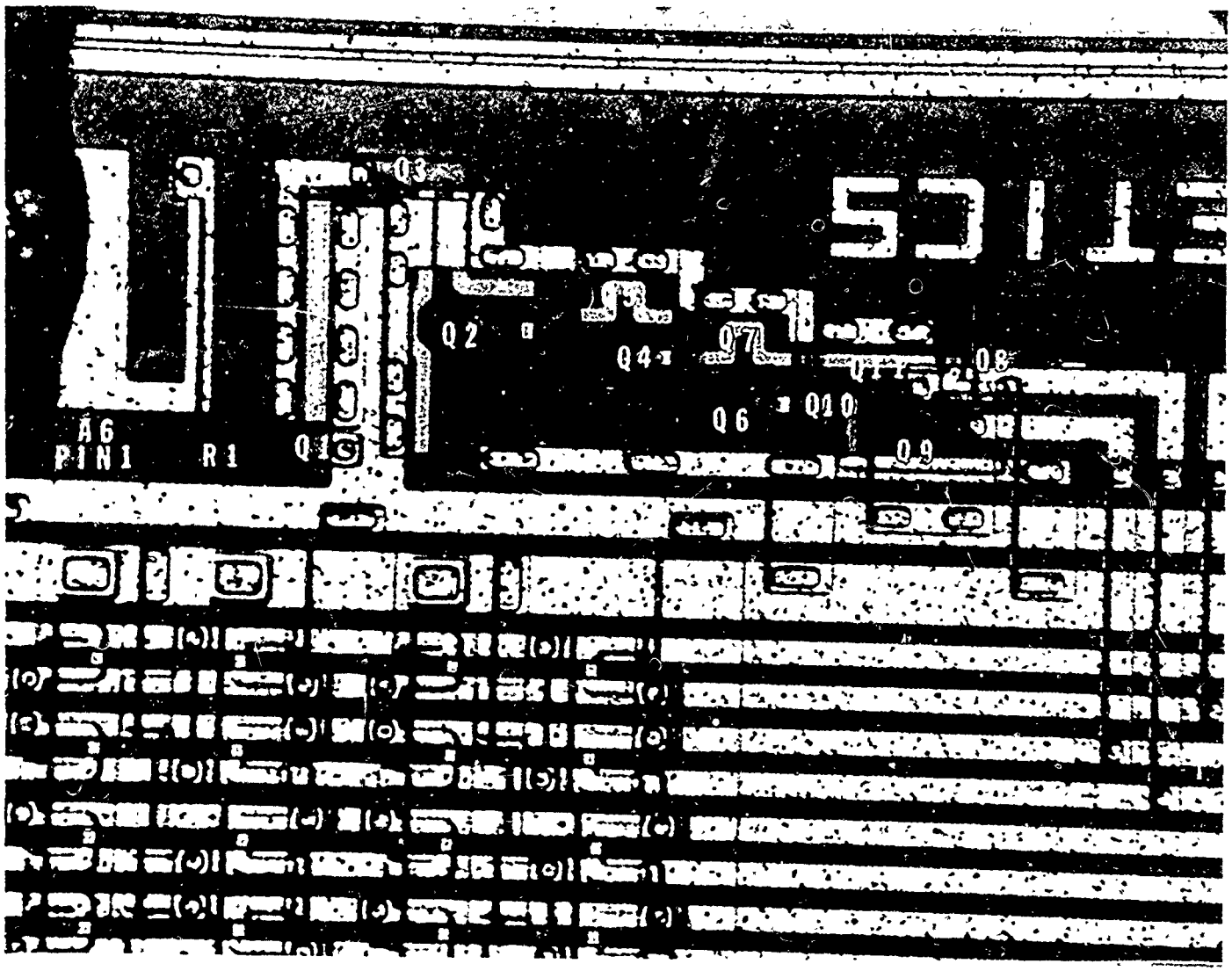


Photo 5-6 Light Photograph of the A6 Column Address Buffer. Mag. - 360X

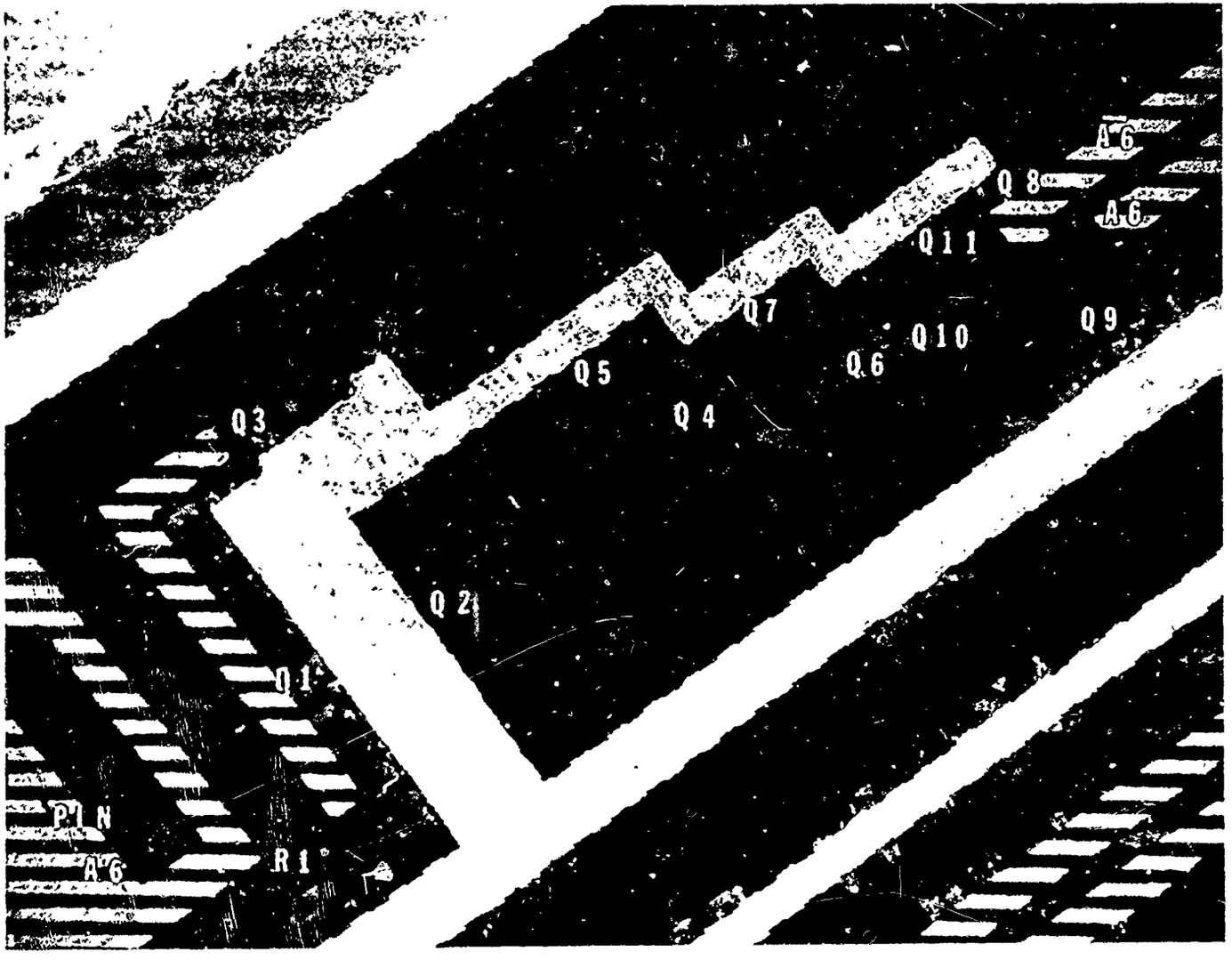


Photo 5-7 Voltage Contrast Micrograph of the A6 Column Address Buffer. 1.5 KV, Mag. - 580X

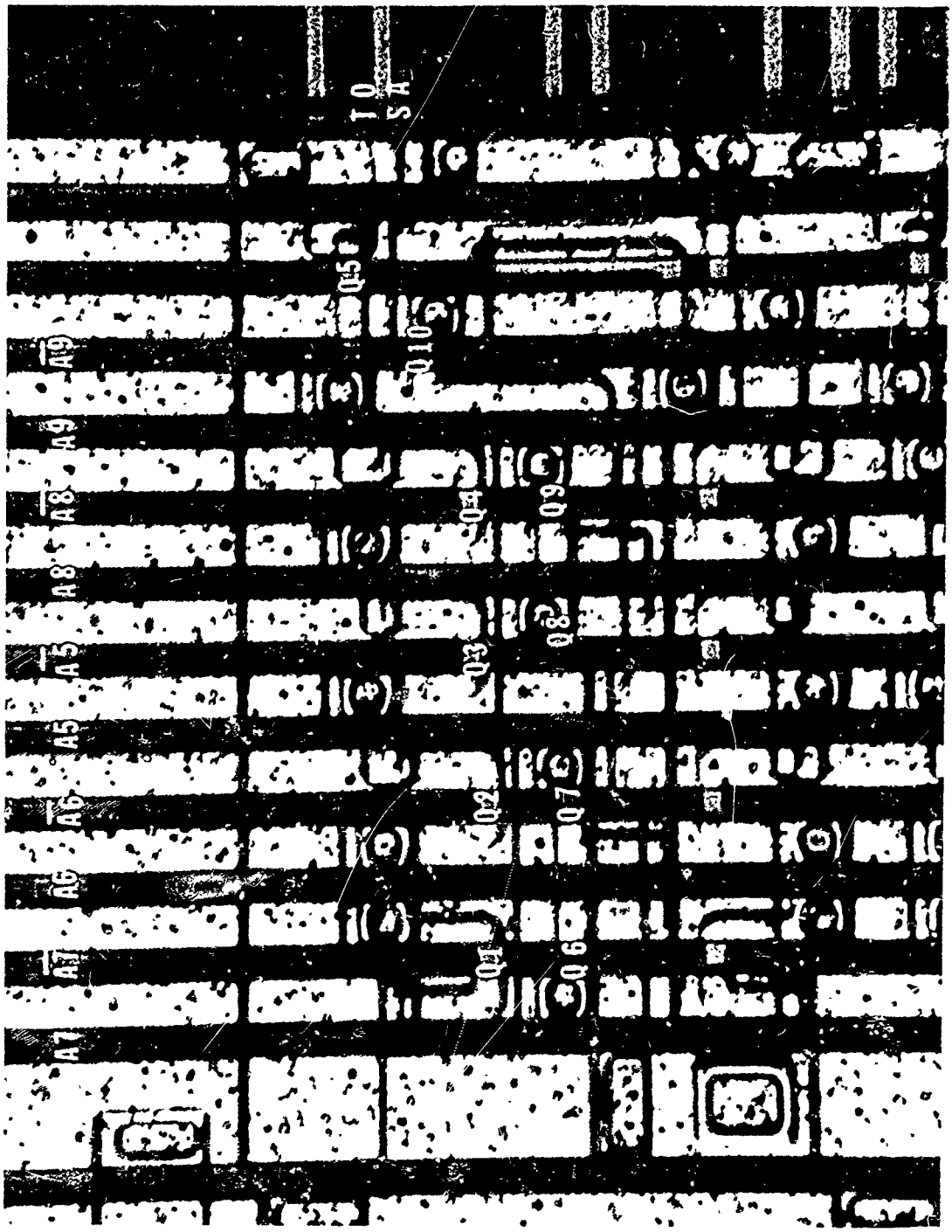


Photo 5-8 Light Photograph of a Column Decode Gate Including Identification of the Column Address Busses. Mag. - 580X

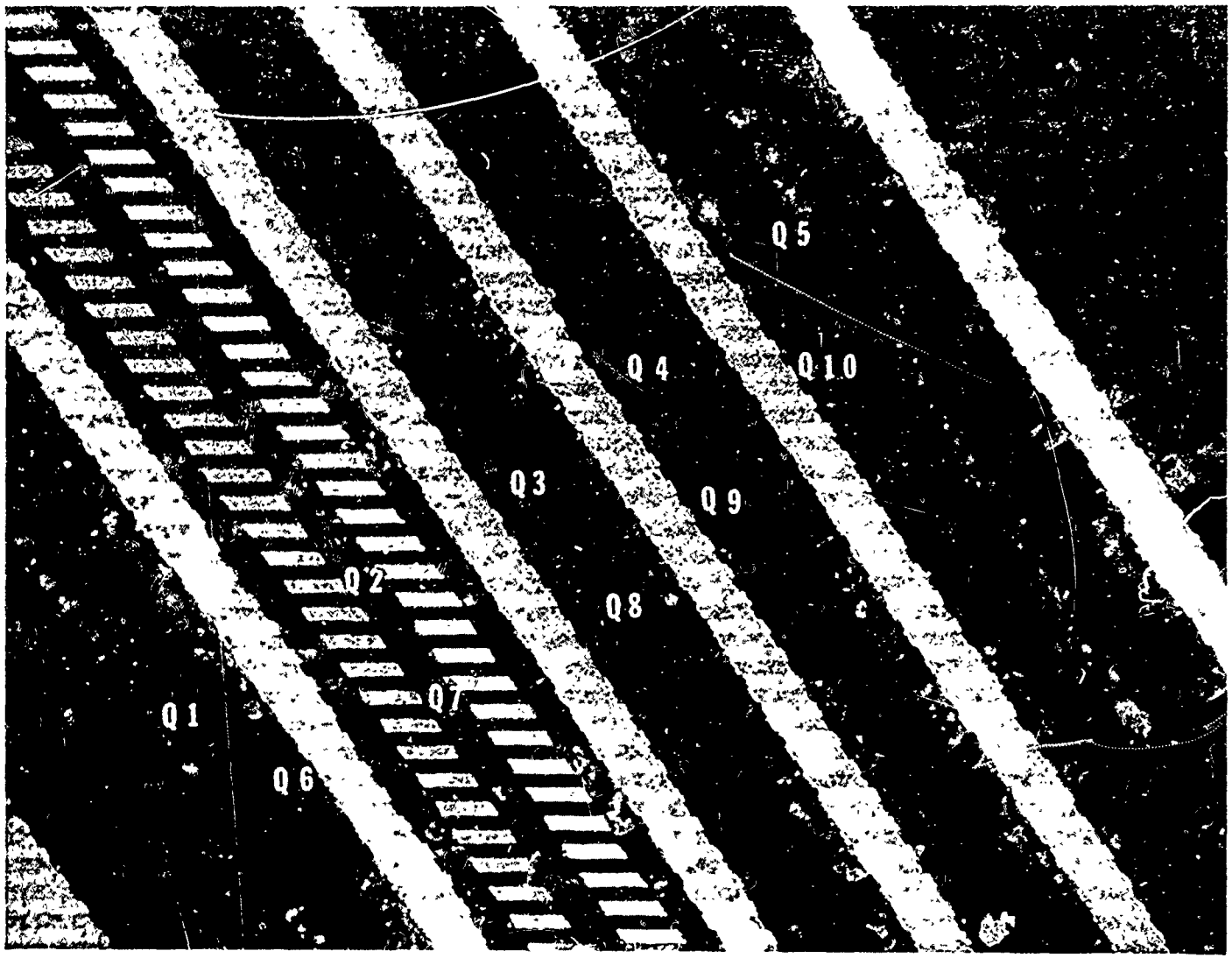


Photo 5-9 Voltage Contrast Micrograph of a Column Decode Gate. 1.5 KV, Mag. - 690X

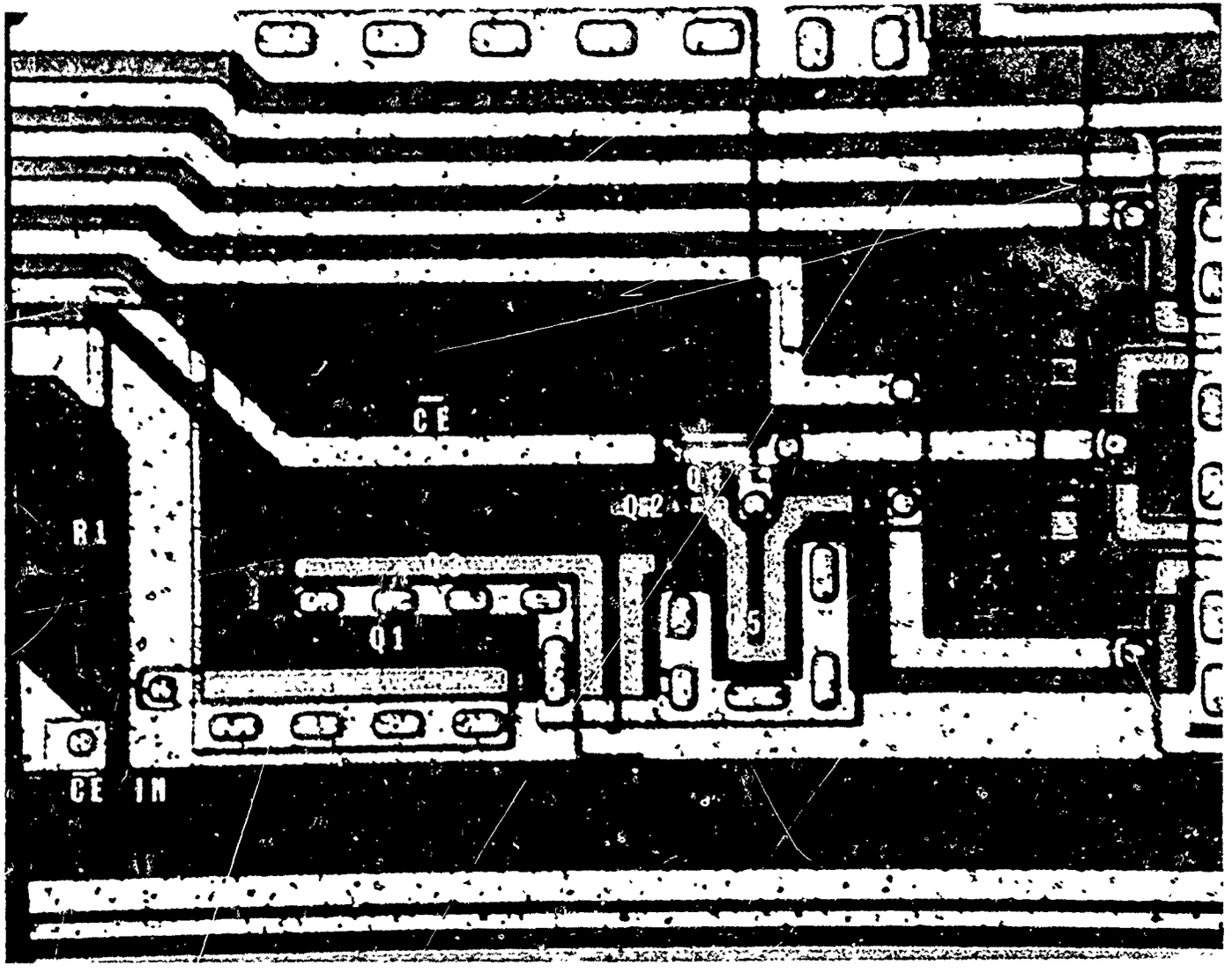


Photo 5-10 Light Photograph of the Chip Enable Circuit. Mag. - 460X

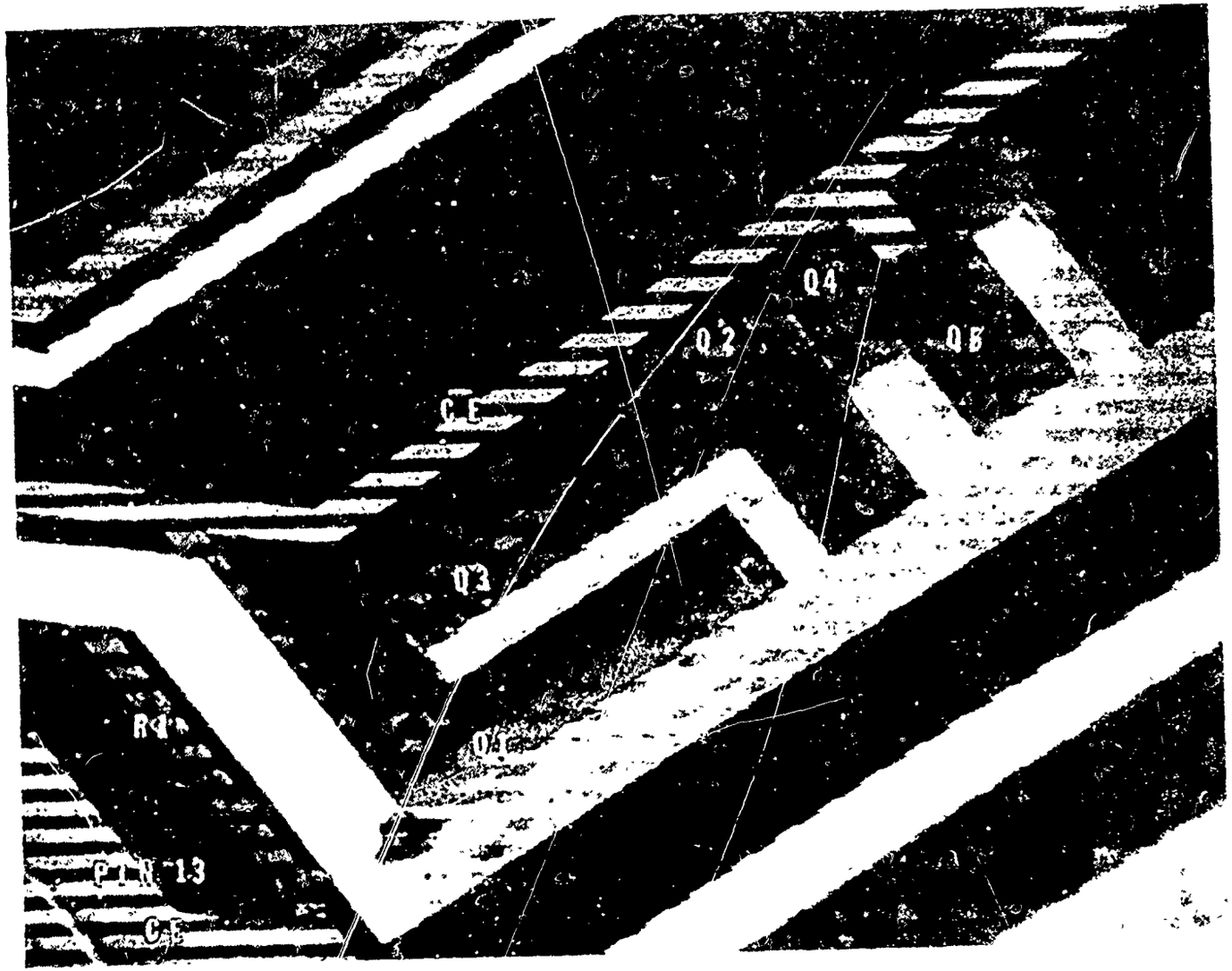


Photo 5-11 Voltage Contrast Micrograph of the Chip Enable Circuit. 1.5 KV, Mag. - 690X

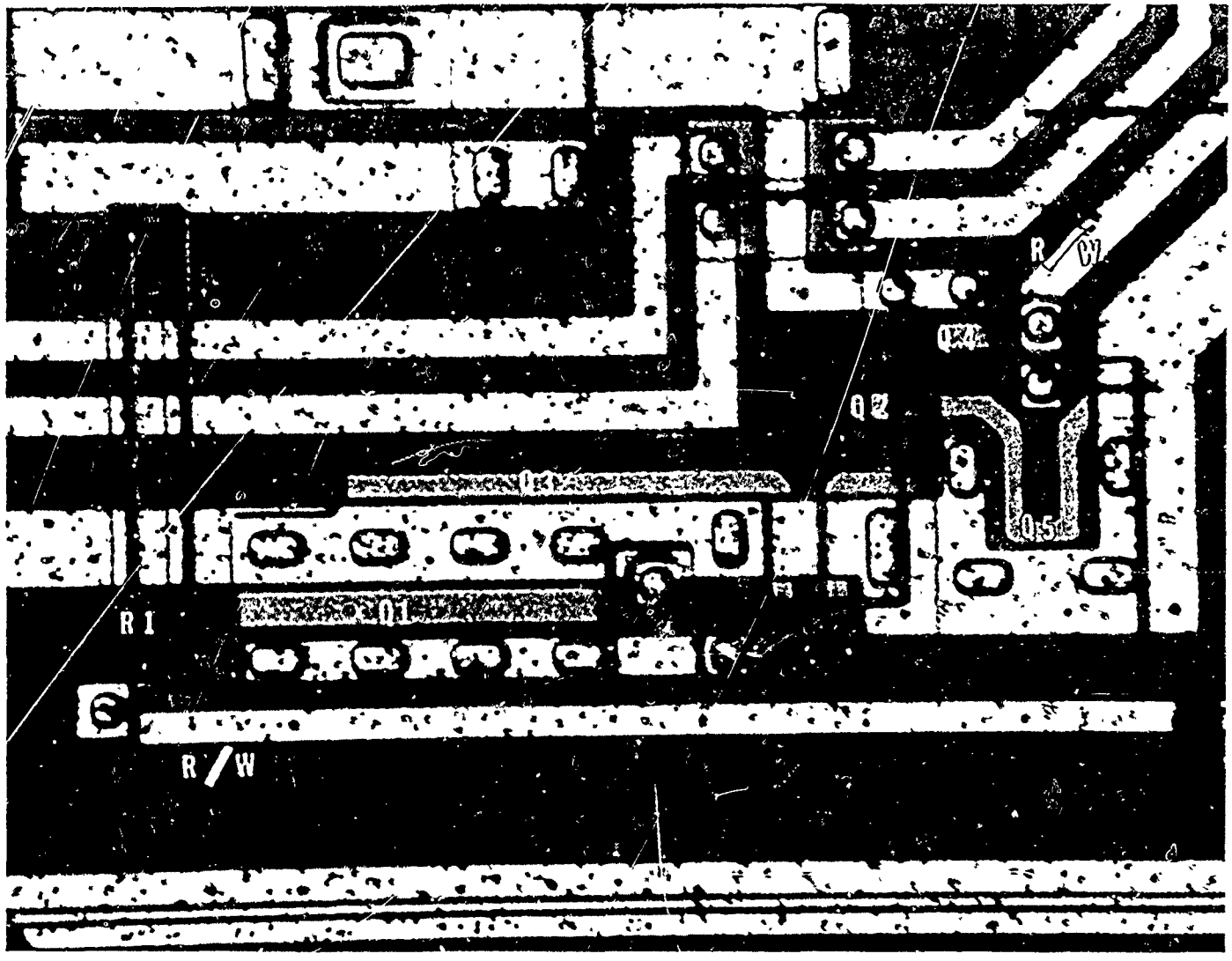


Photo 5-12 Light Photograph of the Read/Write Buffer. Mag. - 580X

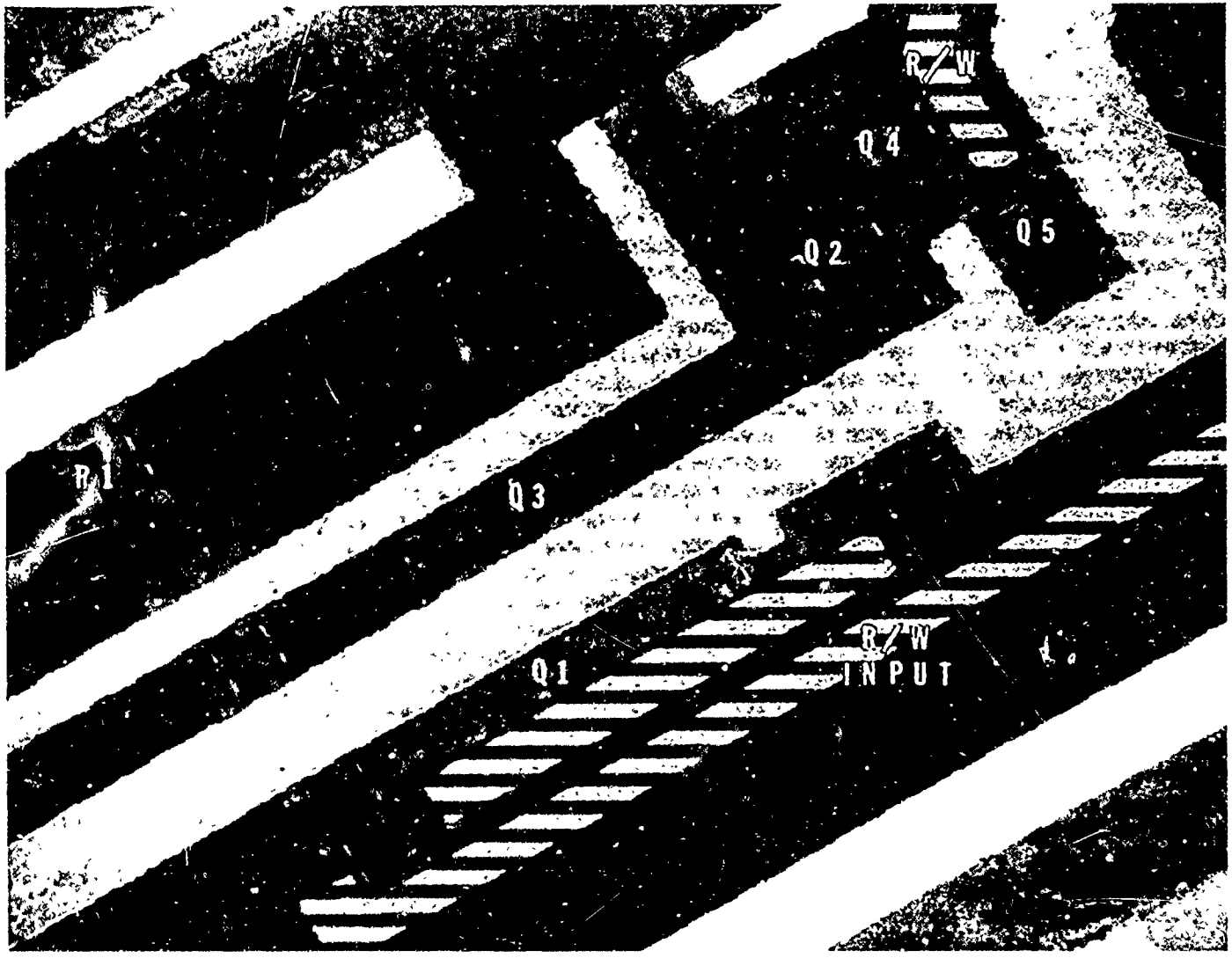


Photo 5-13 Voltage Contrast Micrograph of the Read/Write Buffer. 1.5 KV, Mag. - 690X

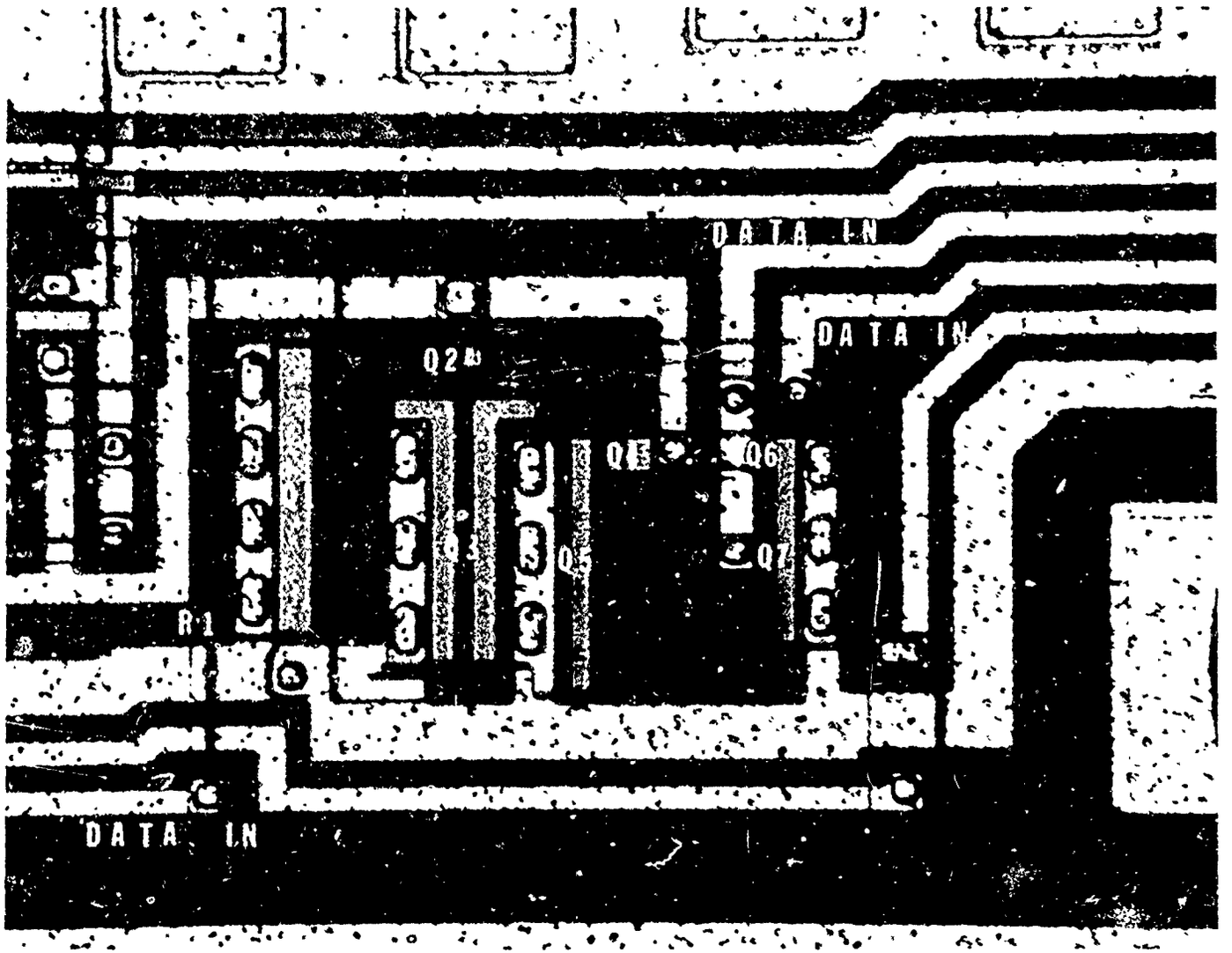


Photo 5-14 Light Photograph of the Data IN Buffer. Mag. - 460X

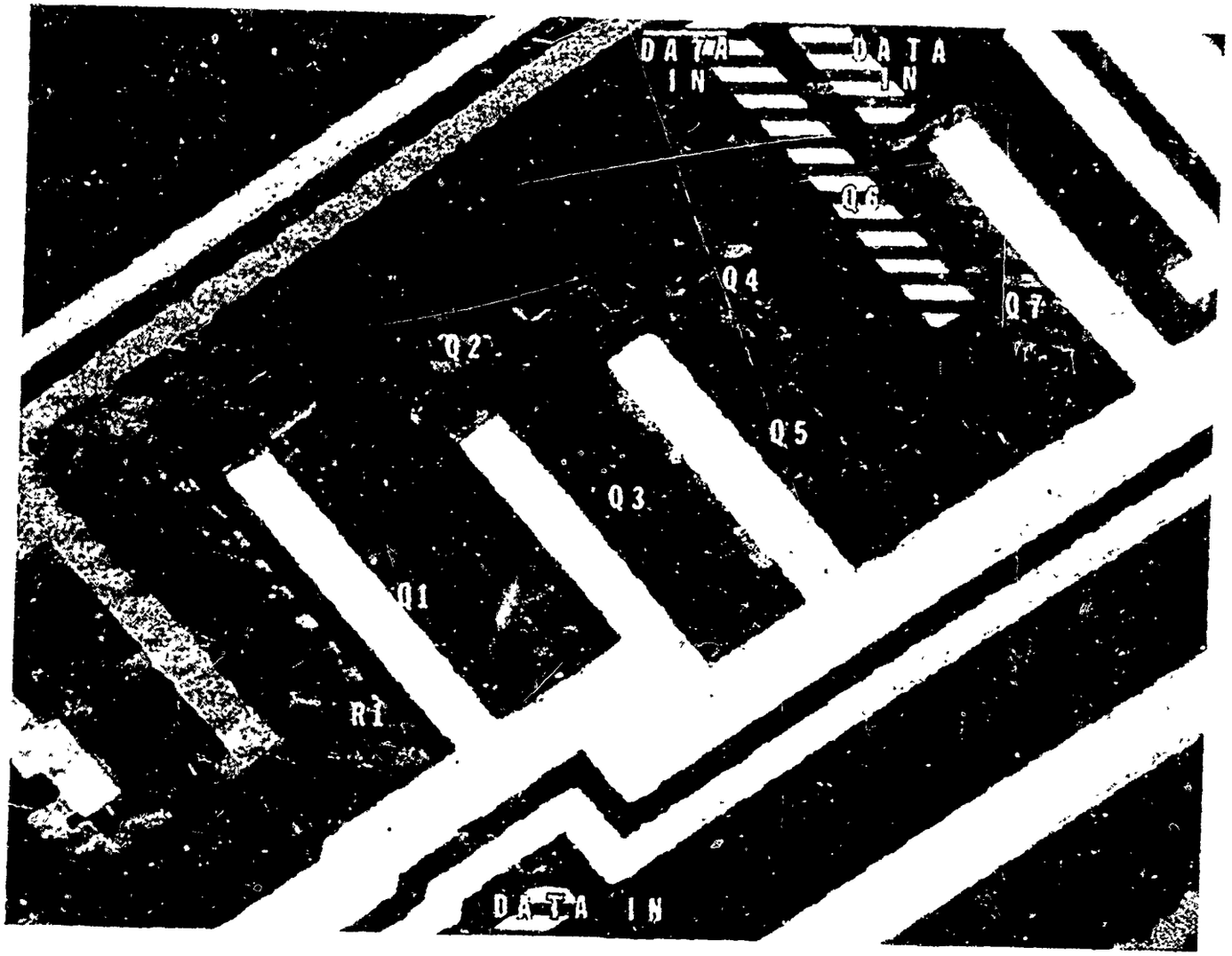


Photo 3-15 Voltage Contrast Micrograph of the Data IN Buffer. 1.5 KV, Mag. - 690X

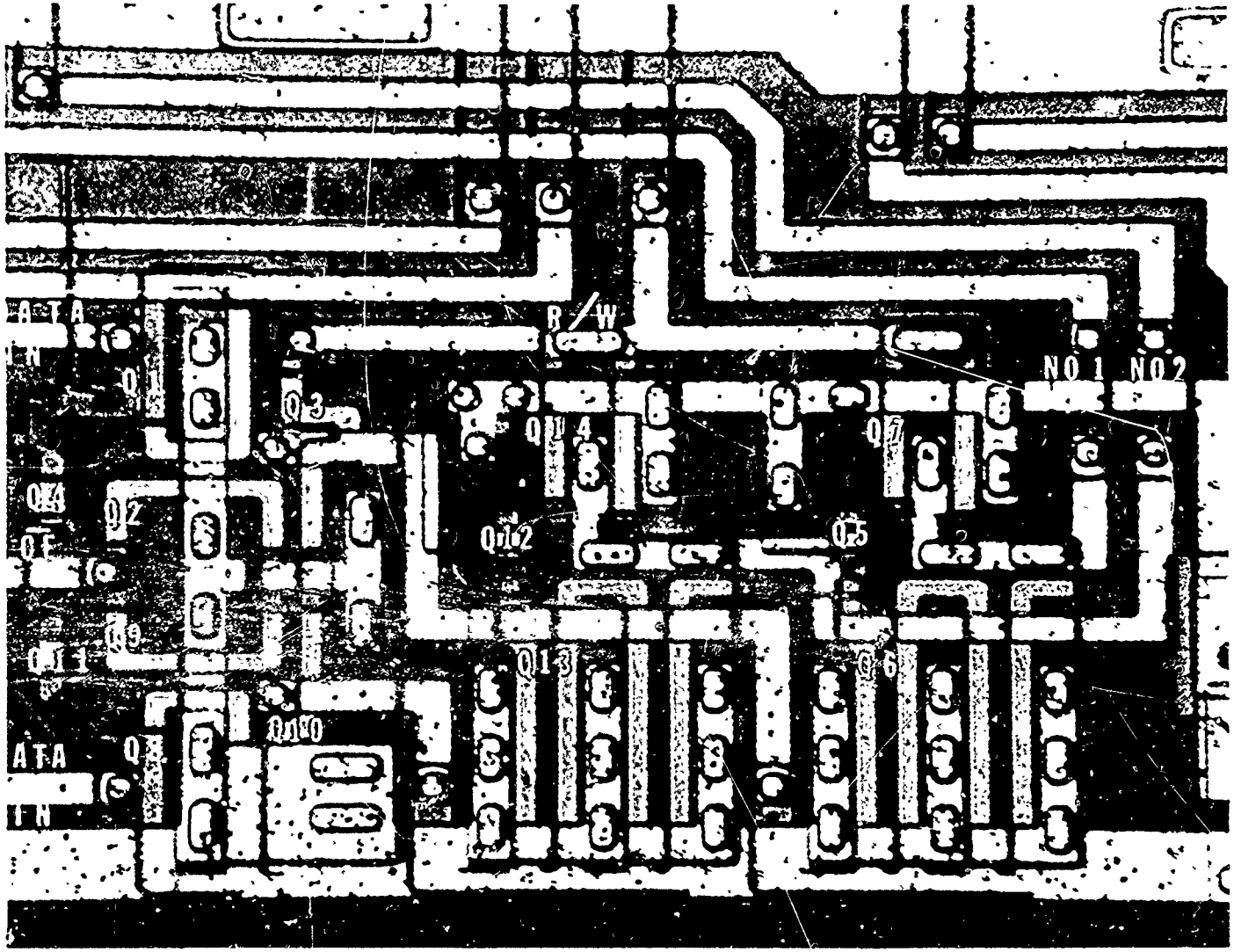


Photo 5-16 Light Photograph of the Input Data Control Circuit. Mag. - 460X

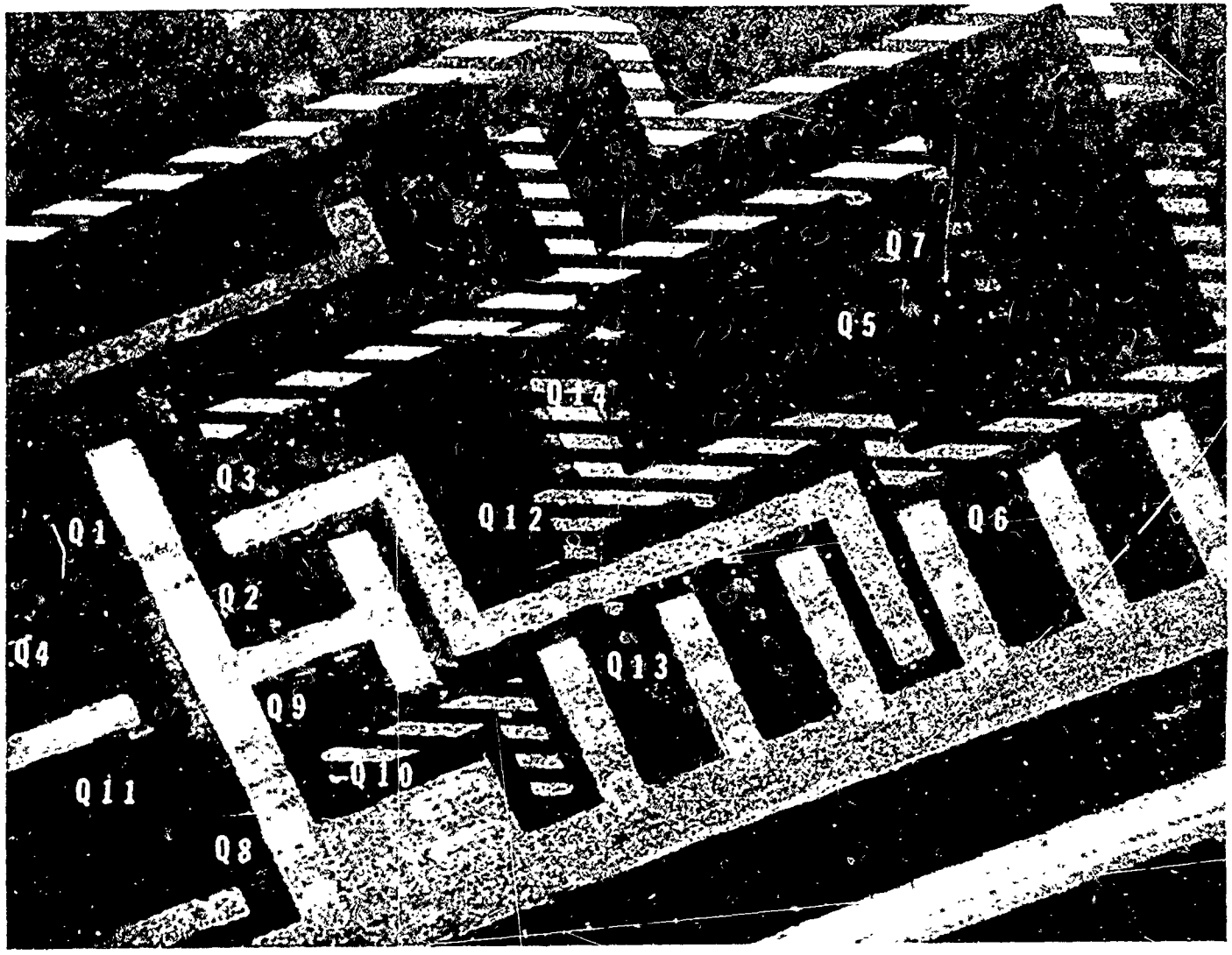


Photo 5-17 Voltage Contrast Micrograph of the Input Data Control Circuit. 1.5 KV, Mag. - 570X

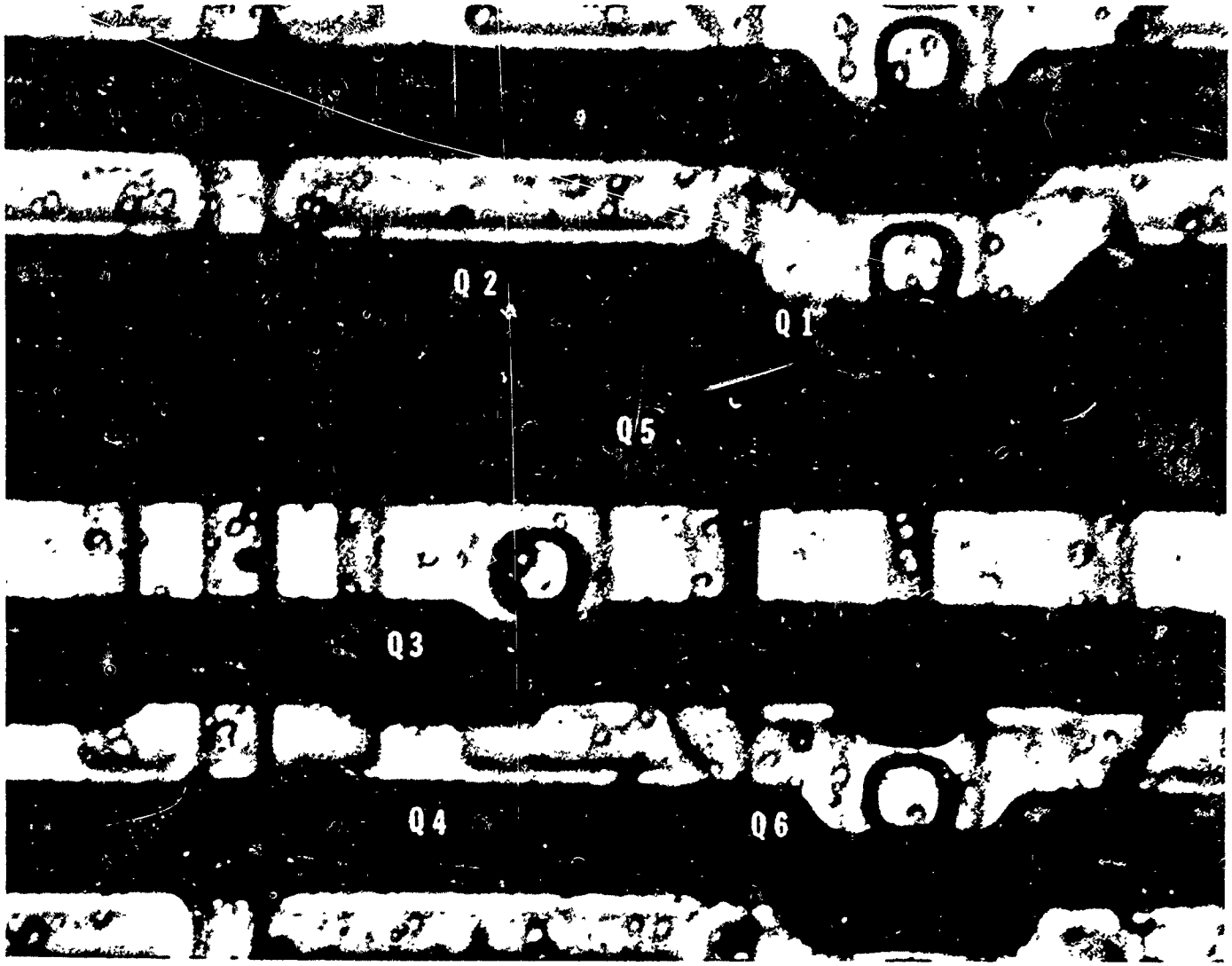


Photo 5-18 Light Photograph of a Typical Memory Cell. Mag. - 1230X

Photo 5-19 Voltage Contrast Micrograph of a Typical Memory Cell. 1.5 KV, Mag. - 1540X

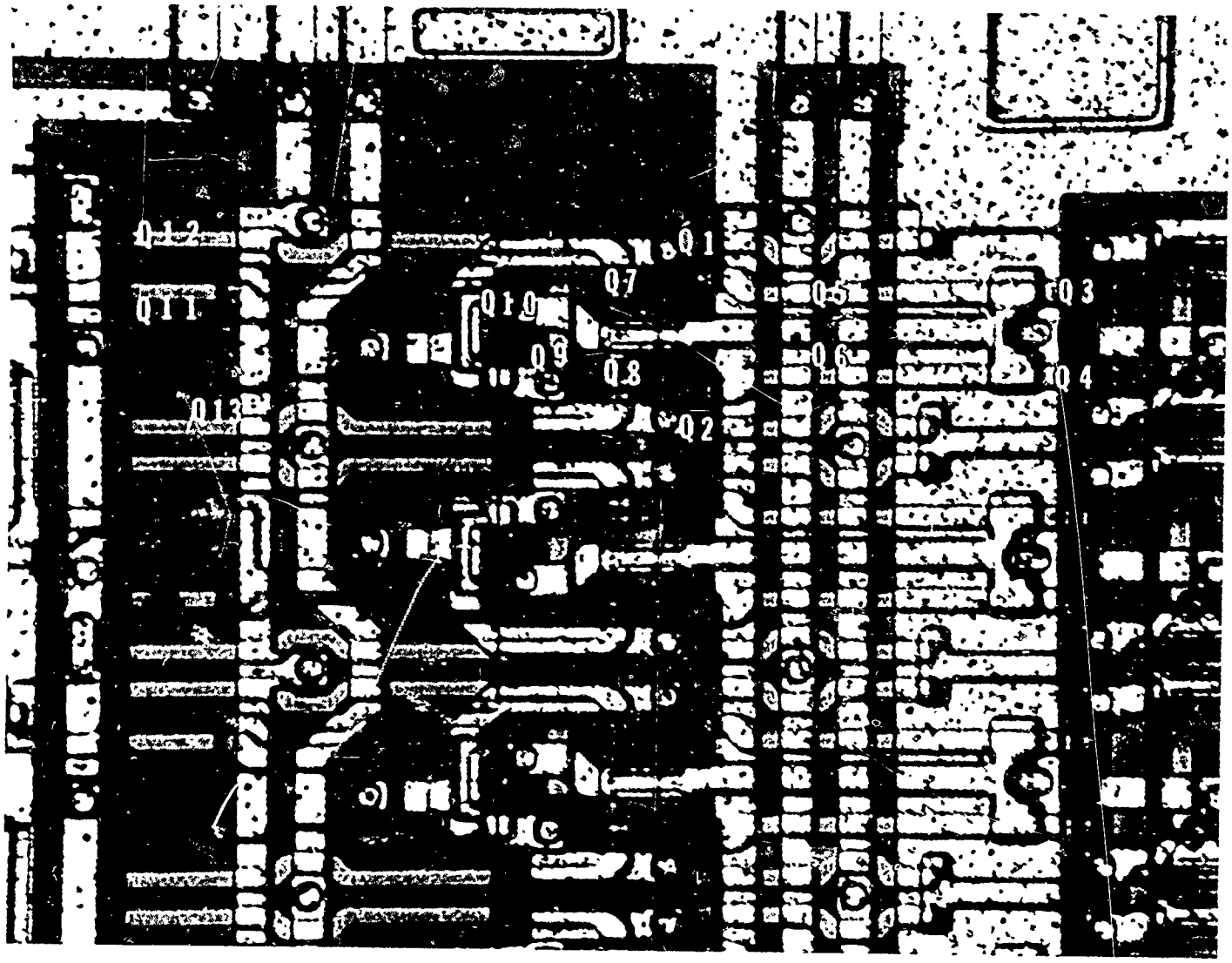


Photo 5-20 Light Photograph of a Sense Amplifier Circuit. Mag. - 460X

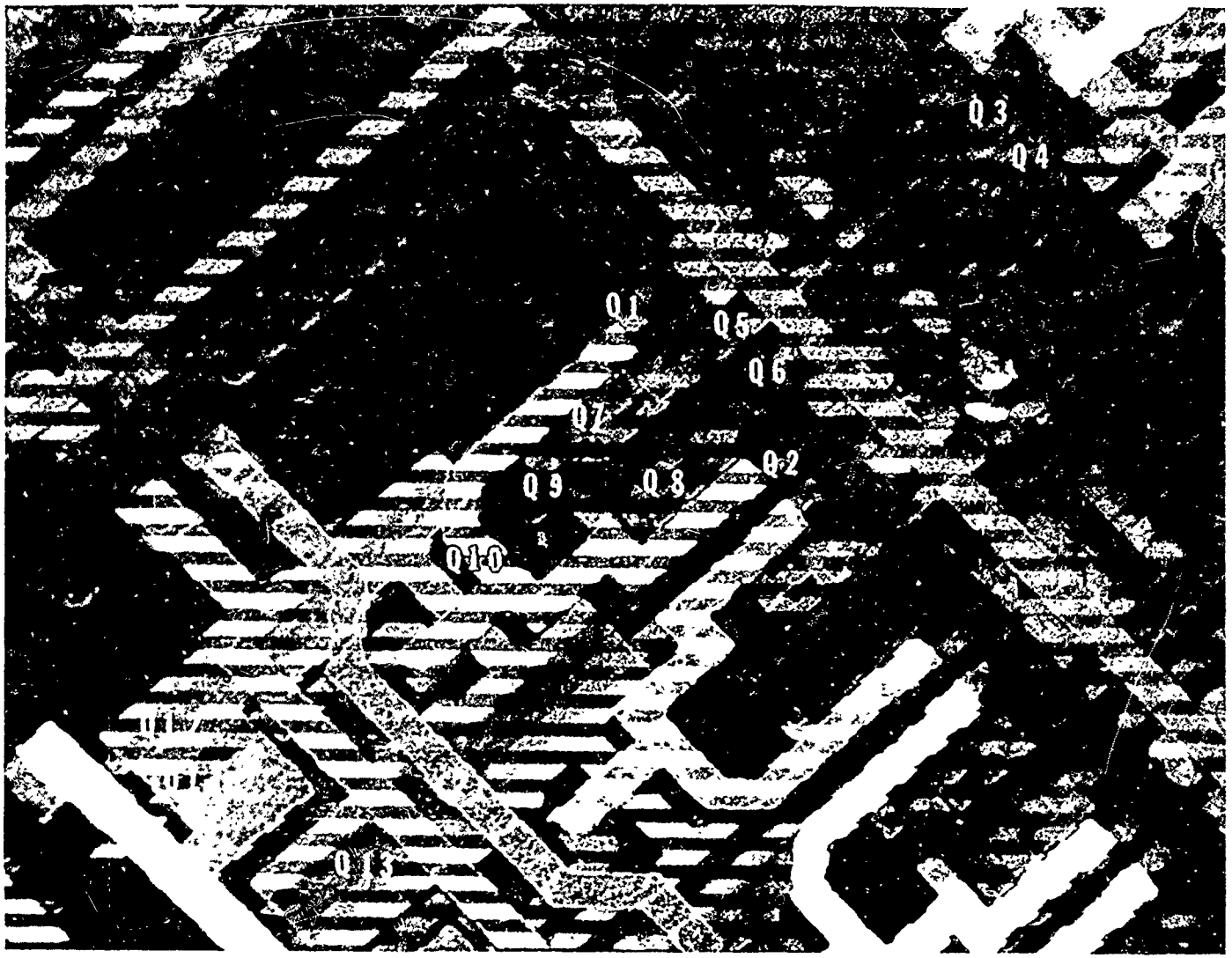


Photo 5-21 Voltage Contrast Micrograph of a Sense Amplifier Circuit. 1.5 KV, Mag. - 610X

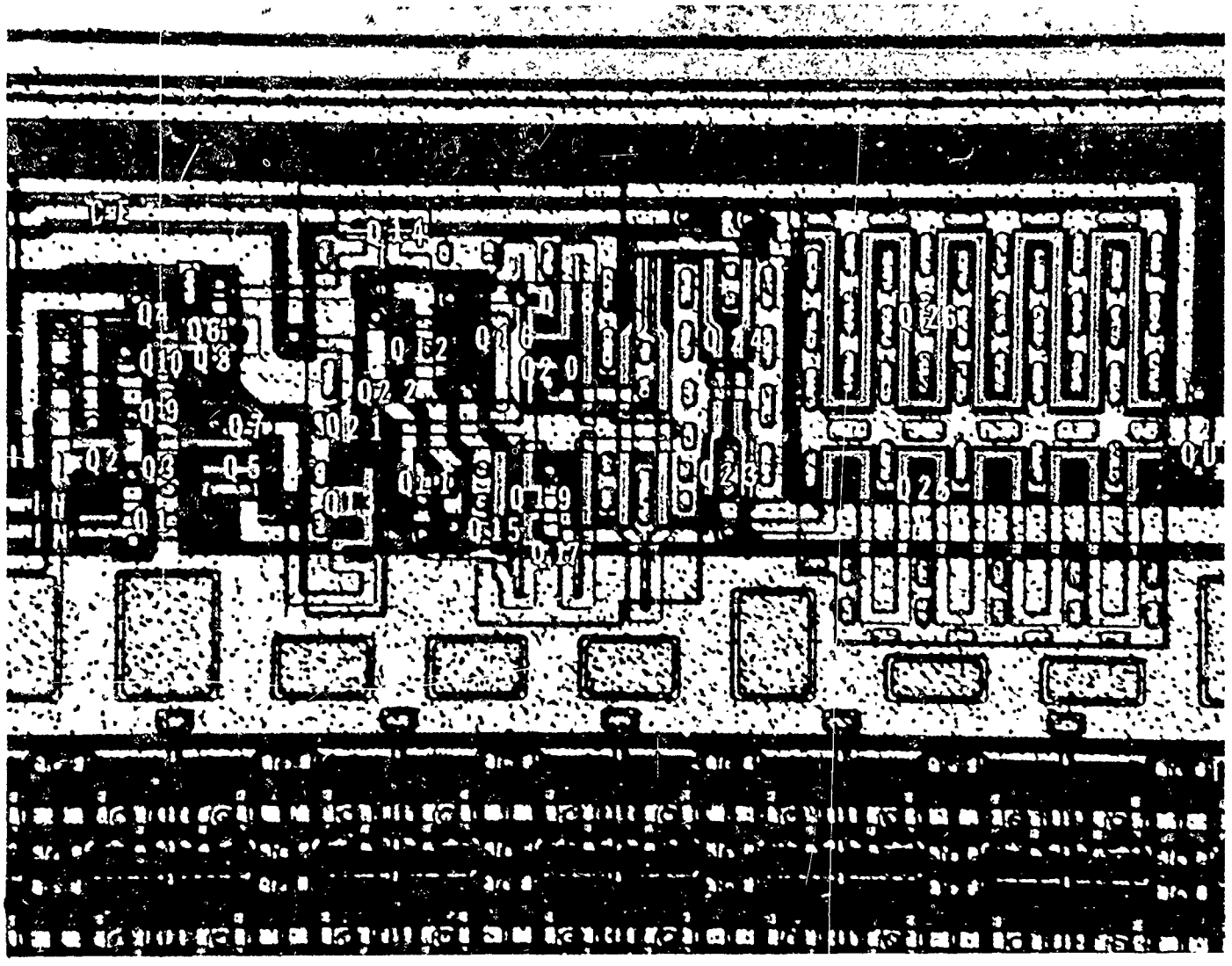


Photo 5-22 Light Photograph of the Data Output Buffer. Mag. - 220X

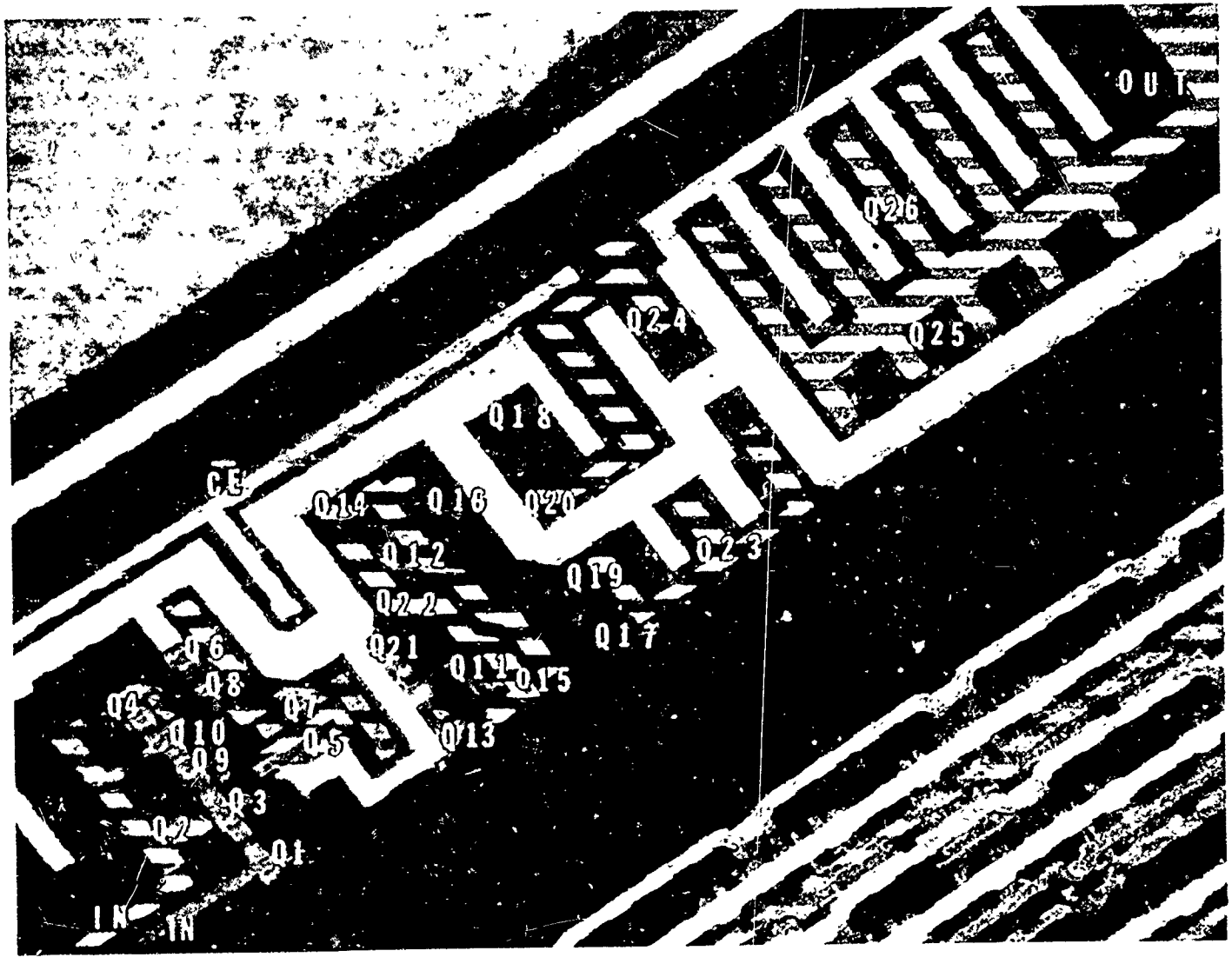


Photo 5-23 Voltage Contrast Micrograph of the Data Output Buffer. 1.5 KV, Mag. - 300X

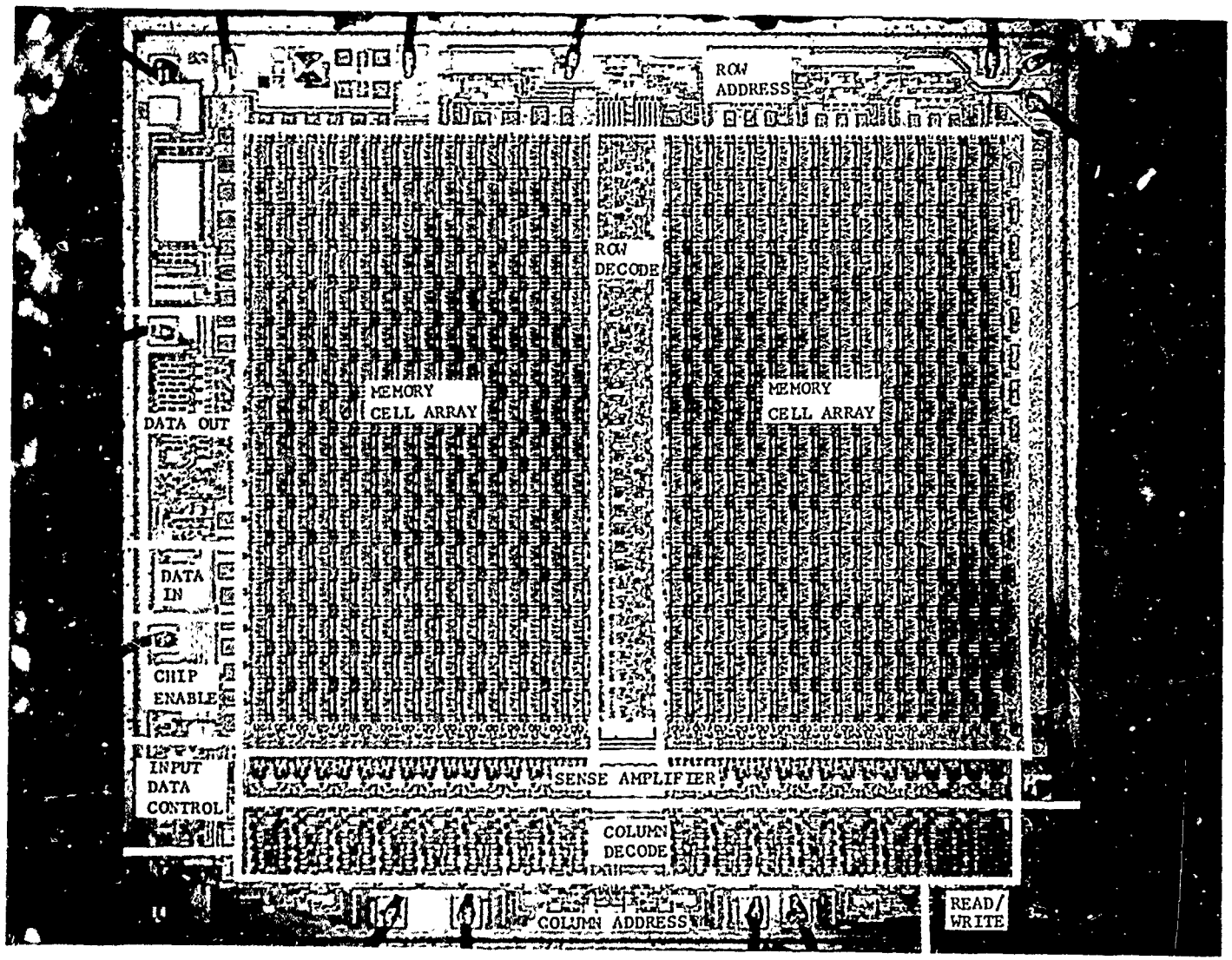


Photo 5-74 Light Photograph of the Entire Die Showing the Functional Blocks. Mag. - 45X

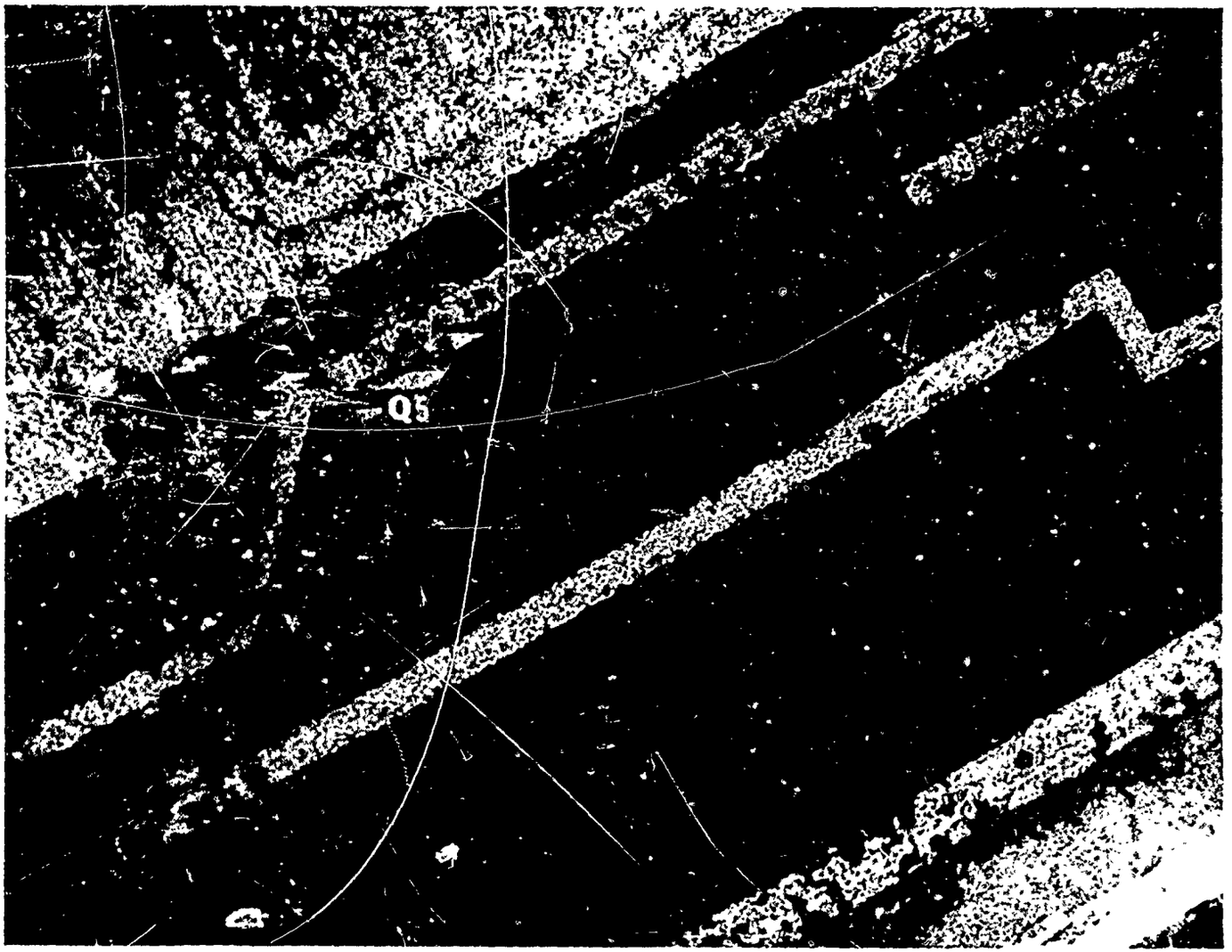


Photo 5-25 Voltage Contrast Micrograph of A2 Row Address Buffer Locating the Area of Circuit Failure. The Candy Stripes Visible Just Above the Q5 Lable is the Signal on the Silicon Gate Element of Q5. 1.5 KV, Mag. ~490X

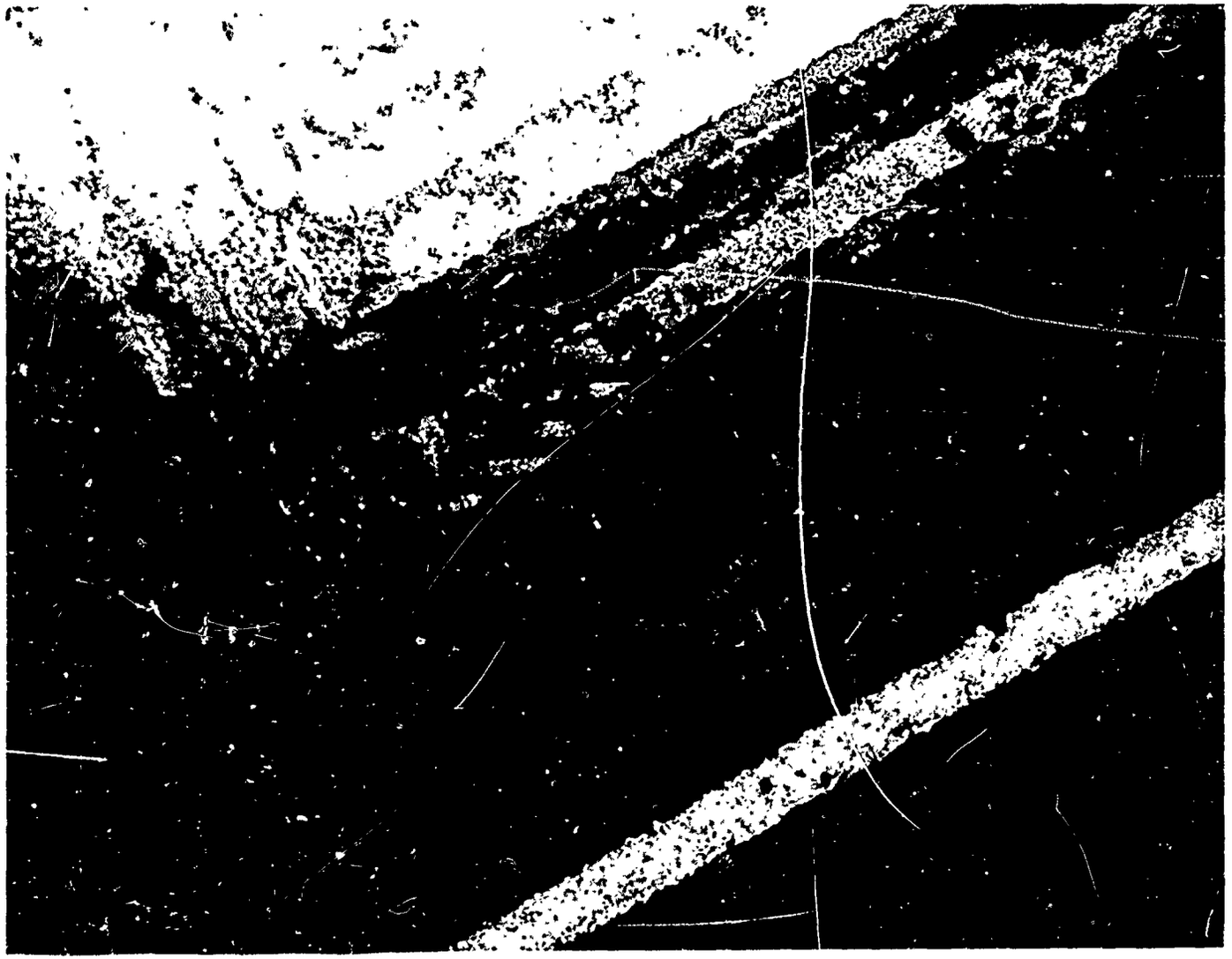


Photo 5-26 Same View as Photo 5-25 at Increased Magnification. In this Photograph a Minimal Voltage Change is Visible in the Q5 Drain Diffusion. 1.5 KV, Mag. - 770X

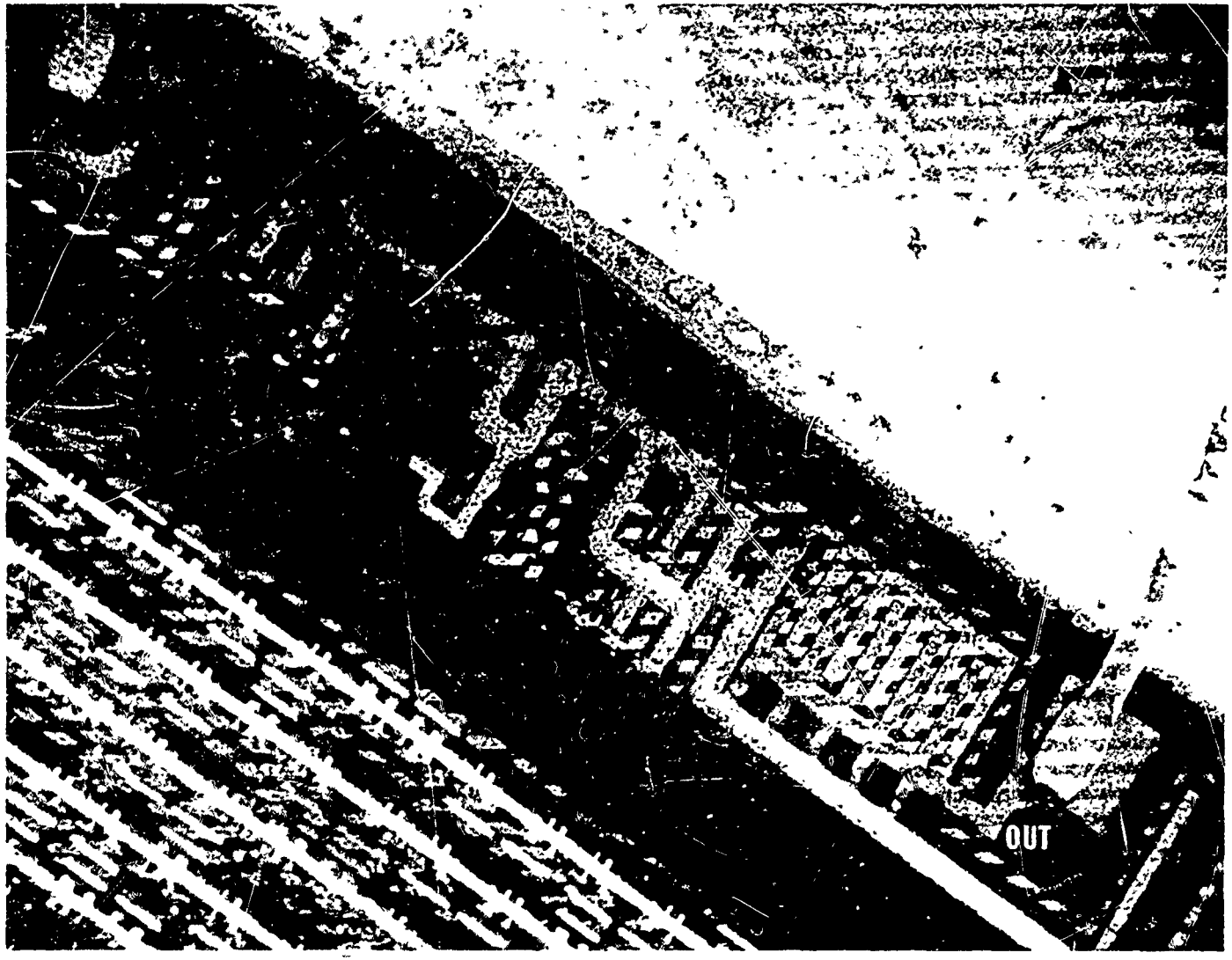


Photo 5-27 Voltage Contrast Micrograph of the Data Output Buffer. This Photograph Shows the Output Does Not go to a High State. 1.5 KV, Mag. - 190X

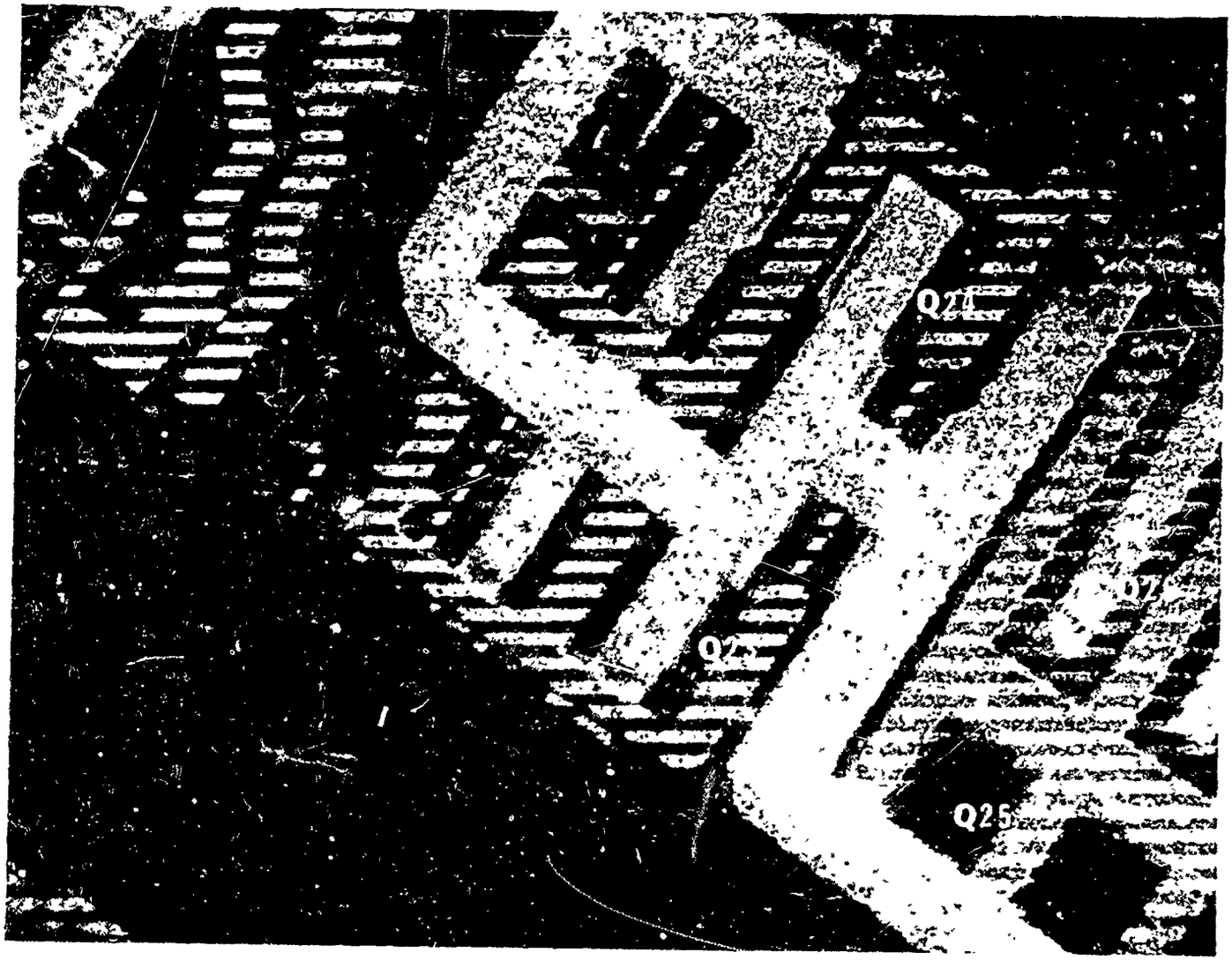


Photo 5-28 Voltage Contrast Micrograph of Data Output Buffer Transistors Q23 and Q24. The Drain of Q24 is Darker than the Drain of Q23. 1.5 KV, Mag. - 610X

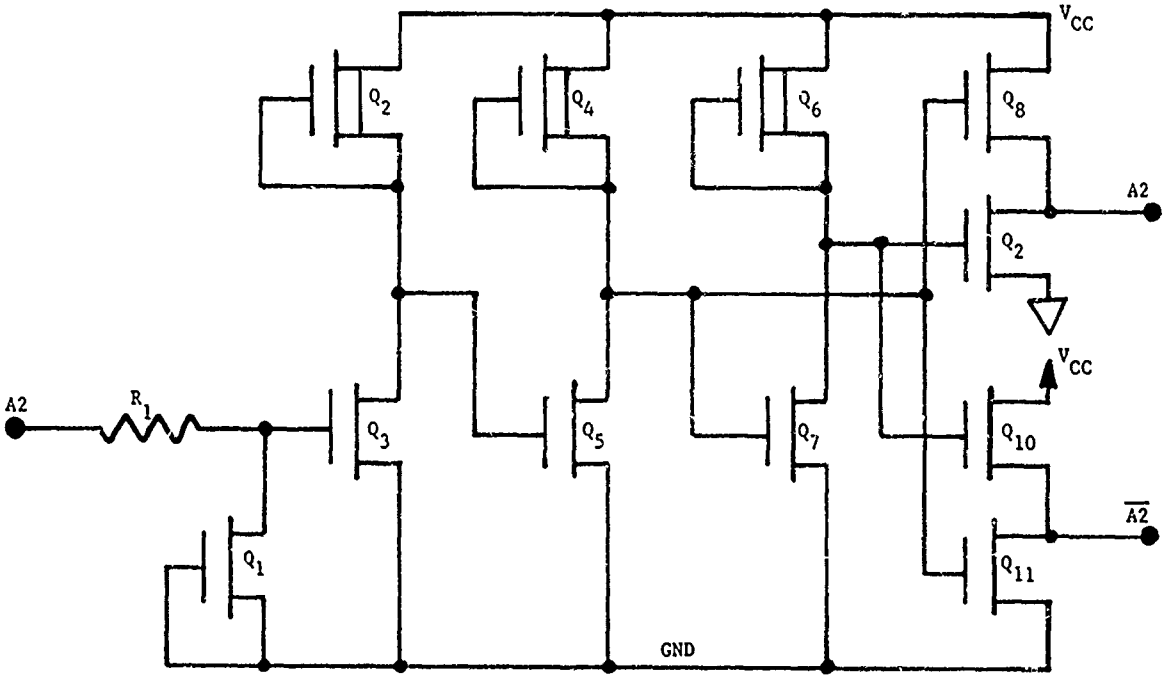


Figure 5-1 Schematic, Row Address Input Buffer

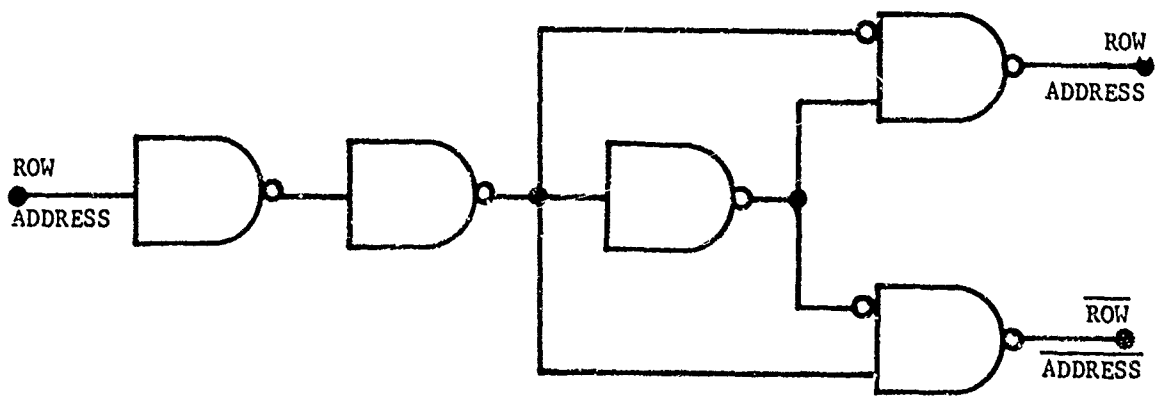


Figure 5-2 Logic Diagram, Row Address Input Buffer

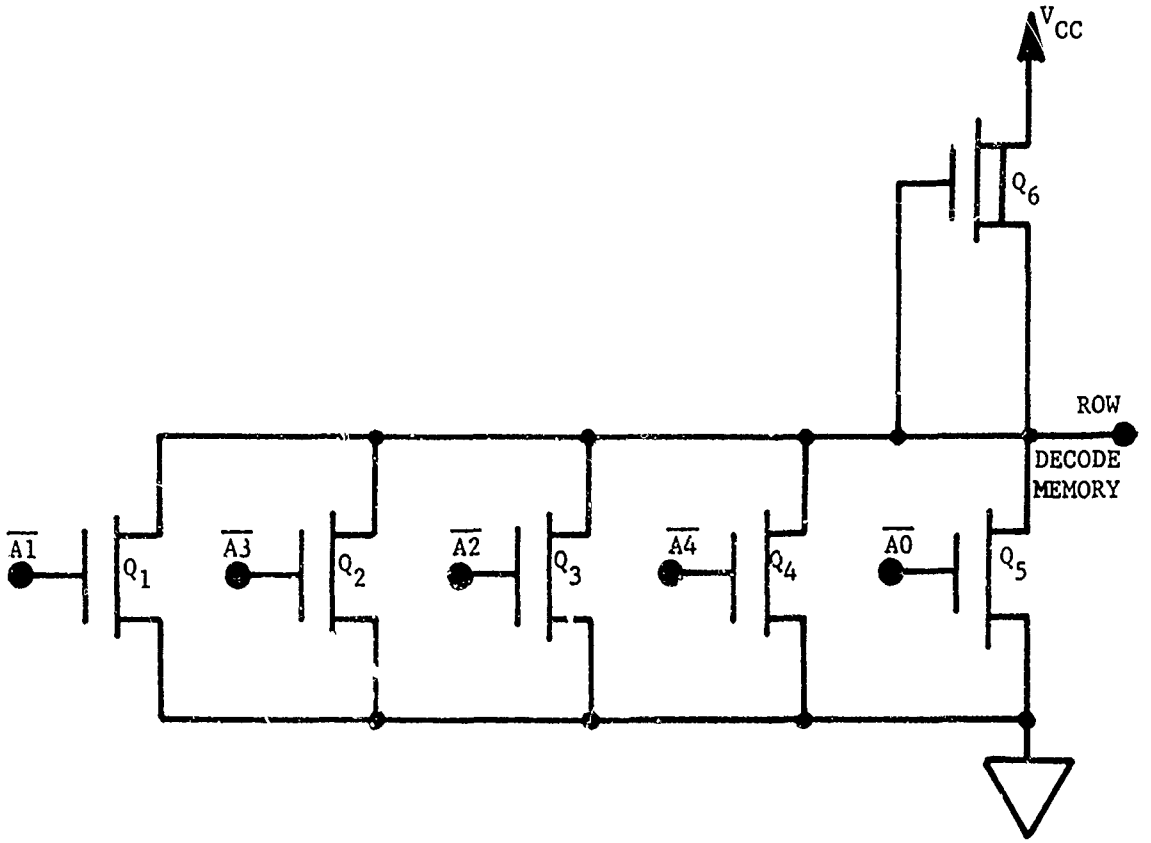


Figure 5-3 Schematic, Row Decode

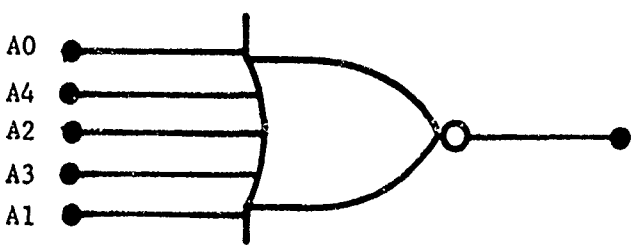


Figure 5-4 Logic Diagram, Row Decode

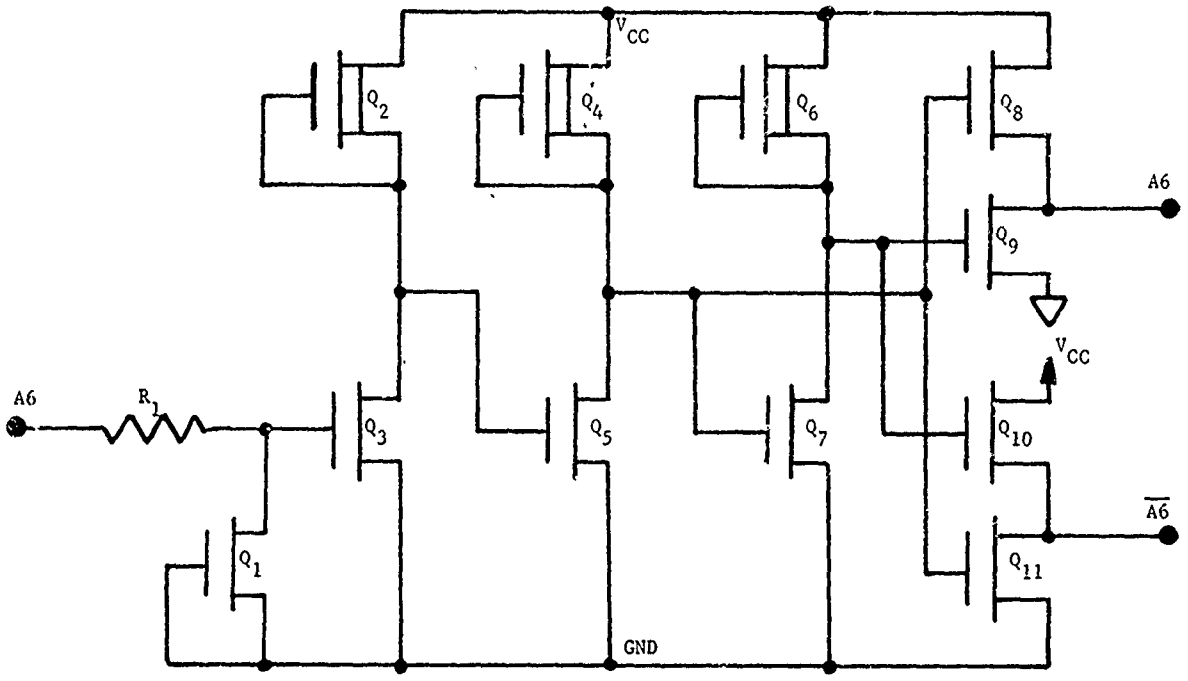


Figure 5-5 Schematic, Column Address Input Buffer

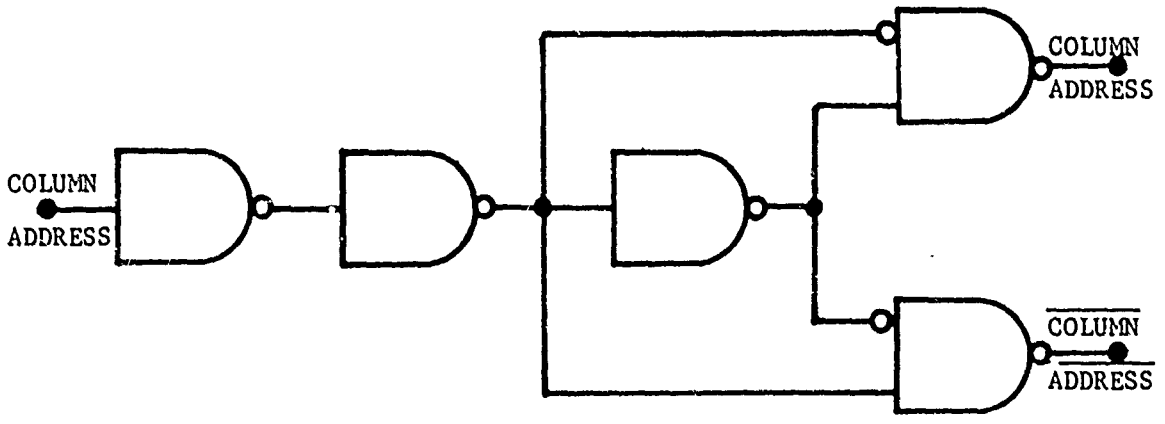


Figure 5-6 Logic Diagram, Column Address Input Buffer

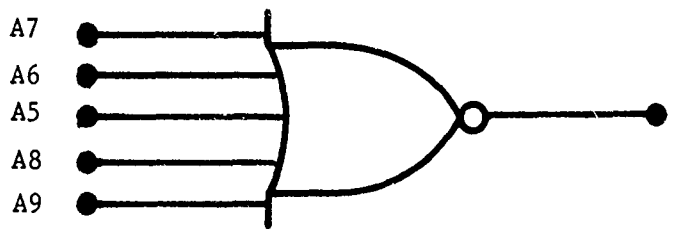


Figure 5-7 Logic Diagram, Column Decode

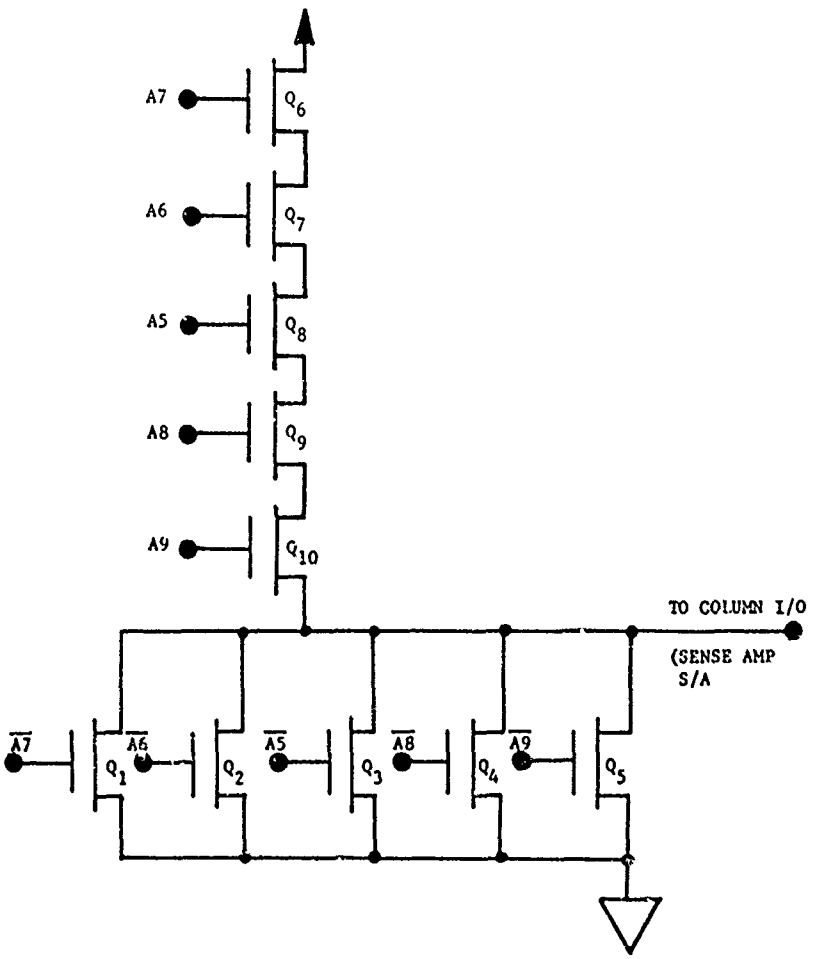


Figure 5-8 Schematic, Column Decode

Figure 5-9 Logic Diagram, Chip Enable

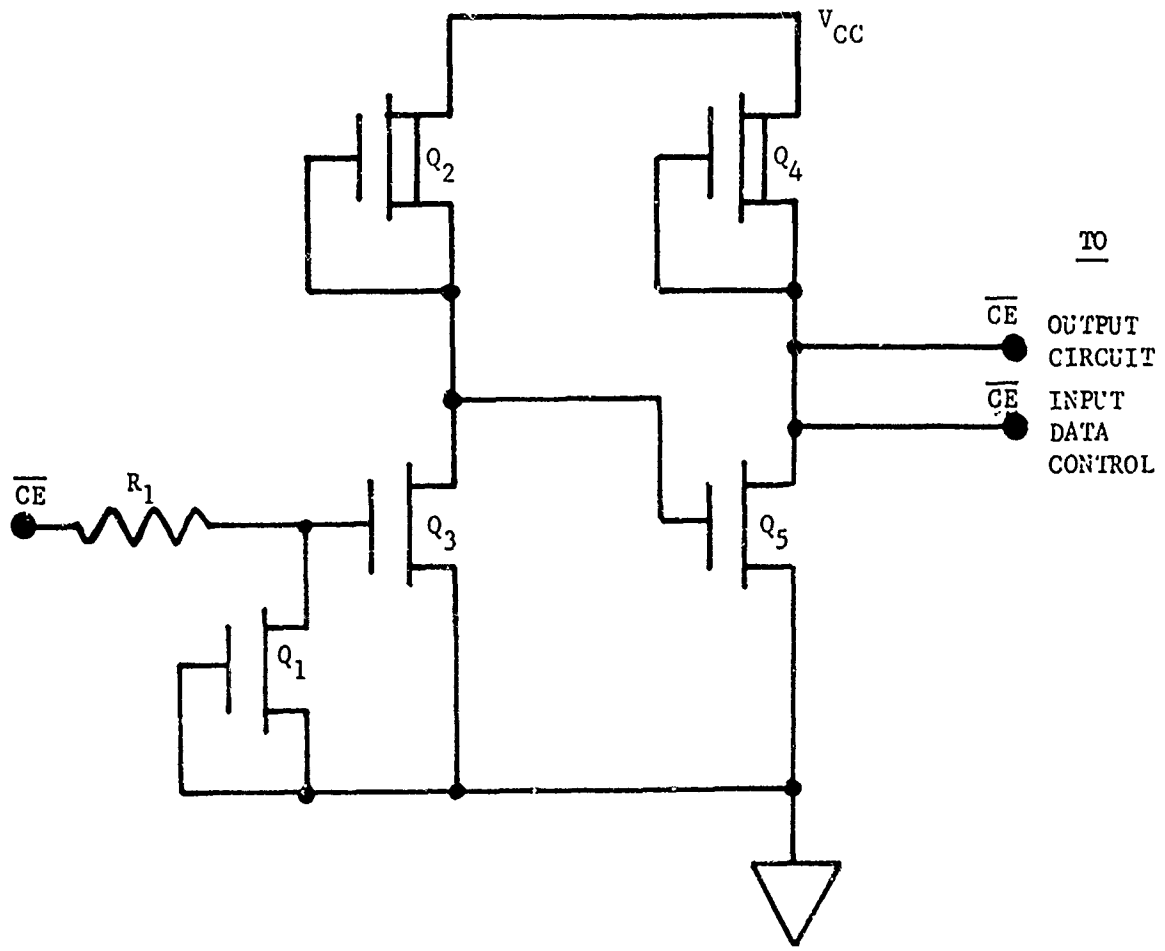


Figure 5-10 Schematic, Chip Enable

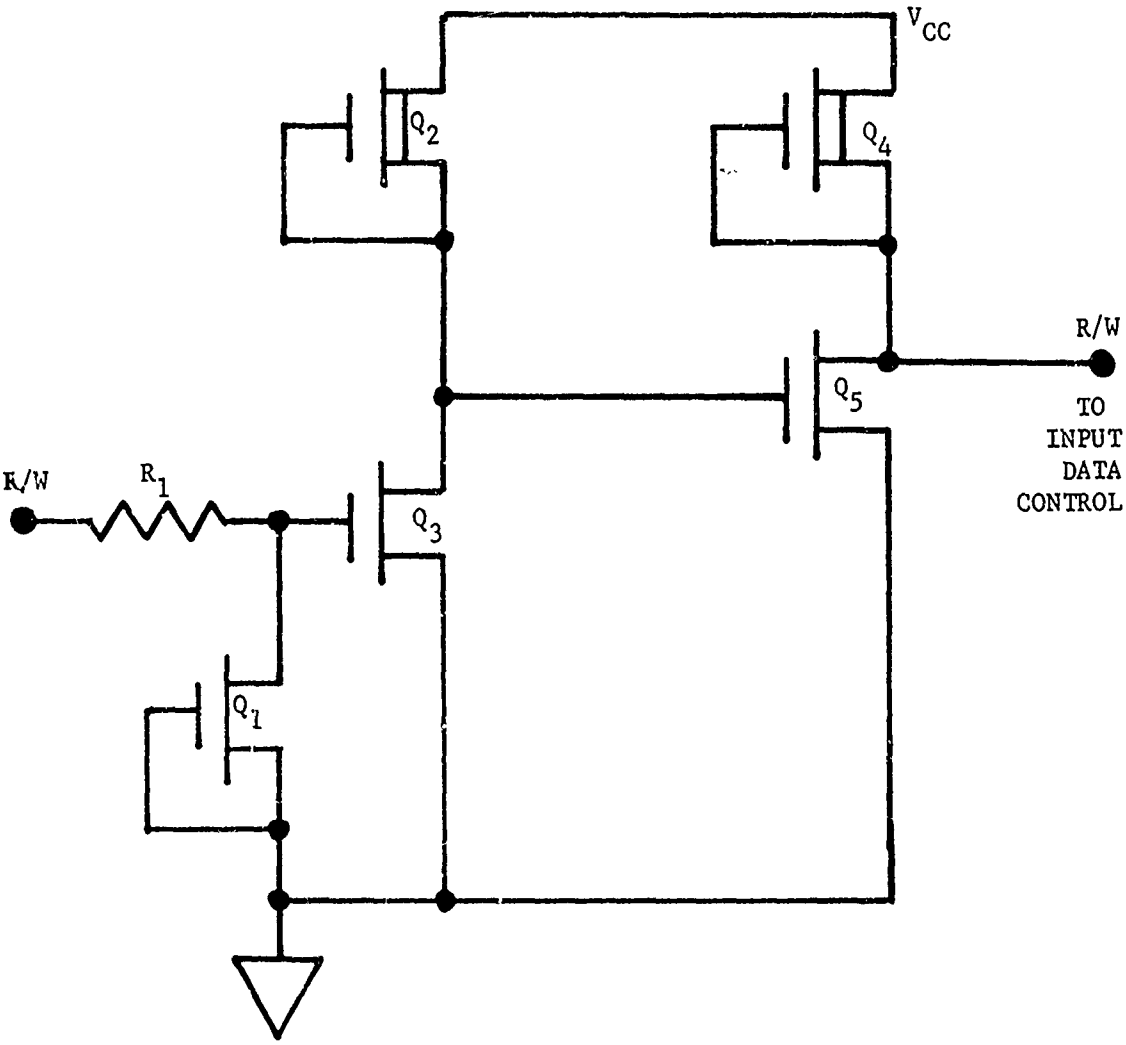


Figure 5-11 Schematic, Read/Write Buffer

Figure 5-12 Logic Diagram, Read/Write Buffer

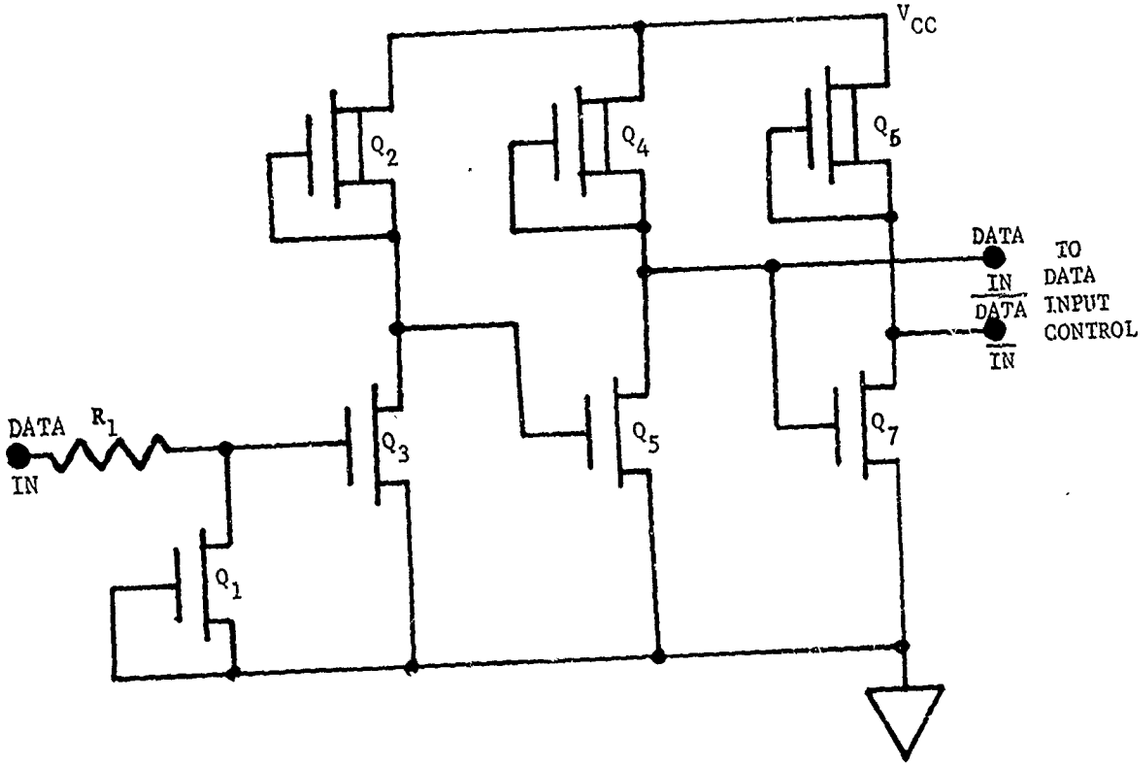


Figure 5-13 Schematic, Data IN Buffer

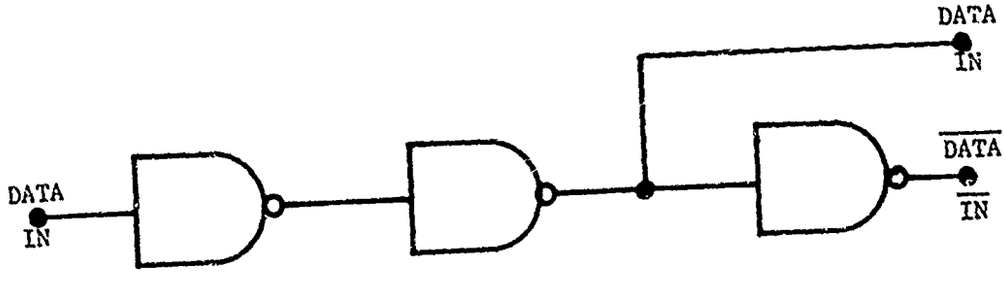


Figure 5-14 Logic Diagram, Data IN Buffer

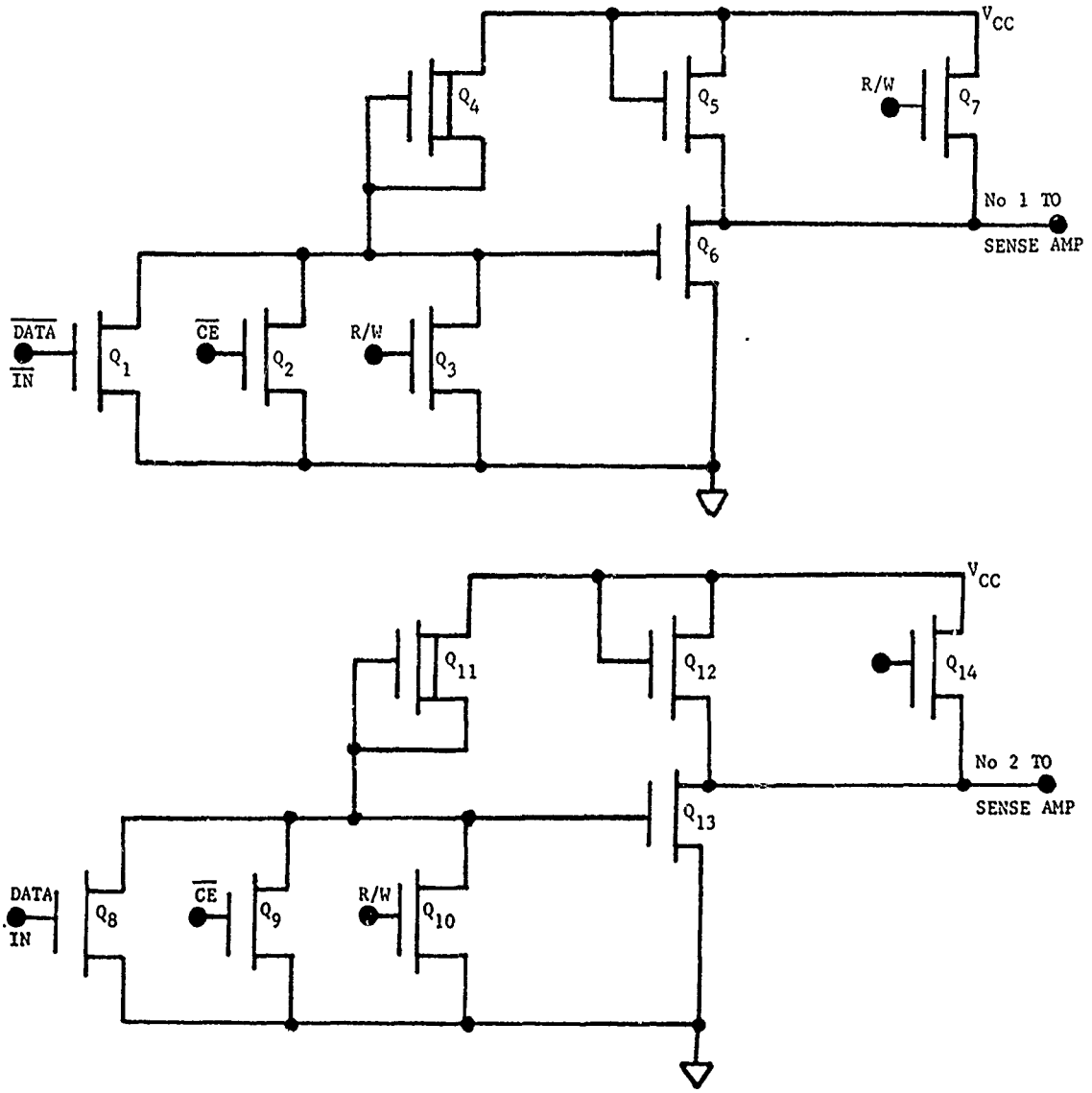


Figure 5-15 Schematic, Input Data Control

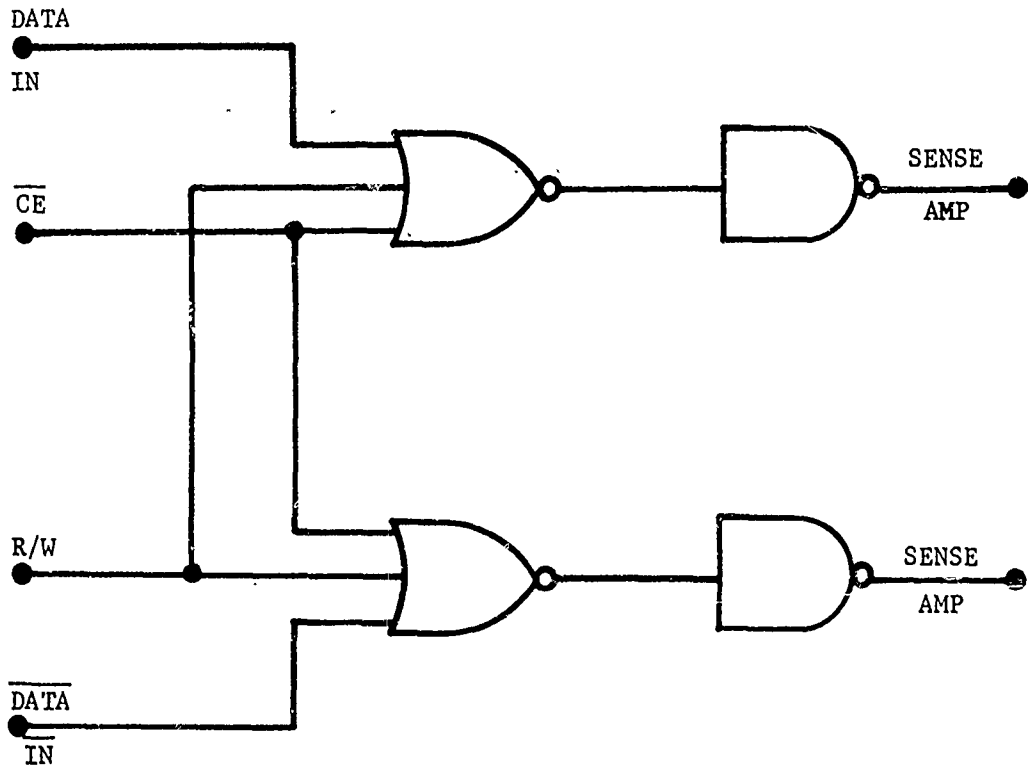


Figure 5-16 Logic Diagram, Input Data Control

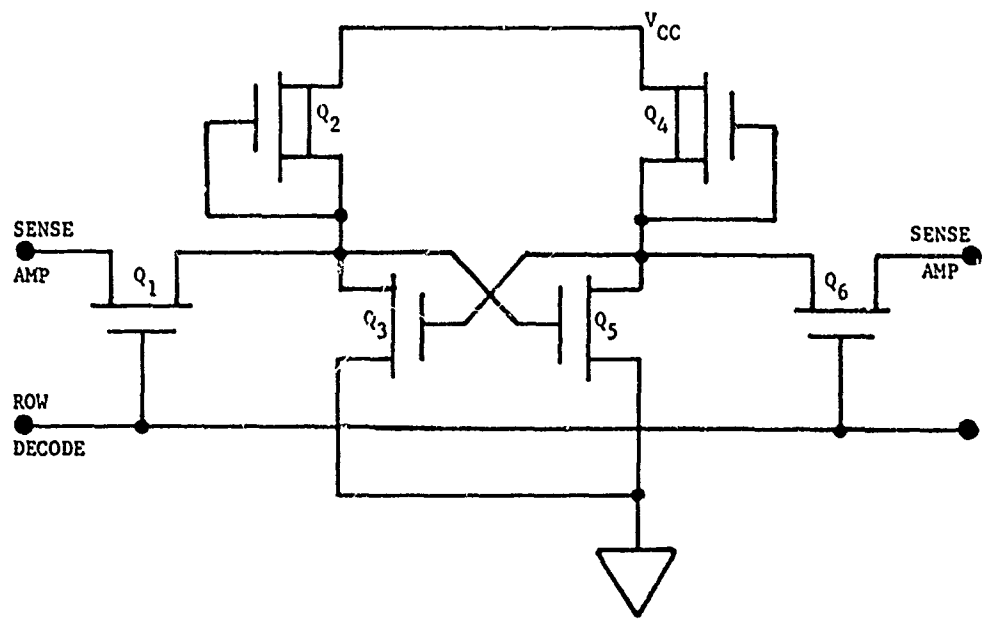


Figure 5-17 Schematic, Memory Cell

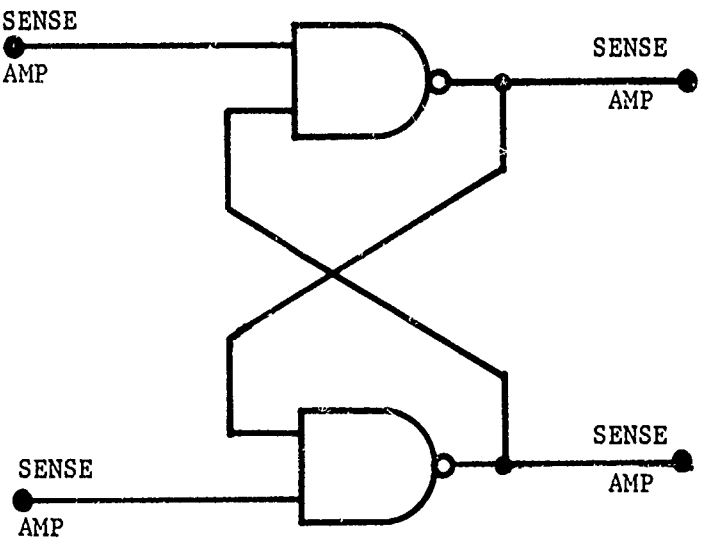


Figure 5-18 Logic Diagram, Memory Cell

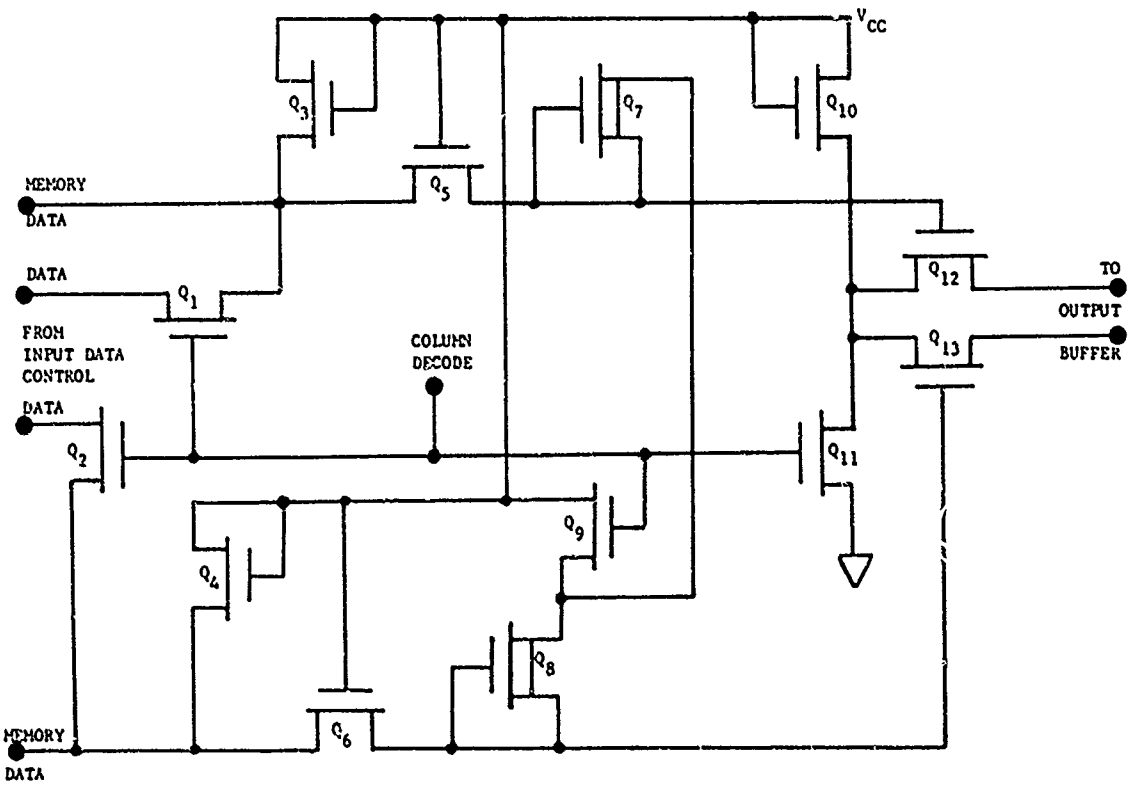


Figure 5-19 Schematic, Sense Amplifier (Data I/O Control)

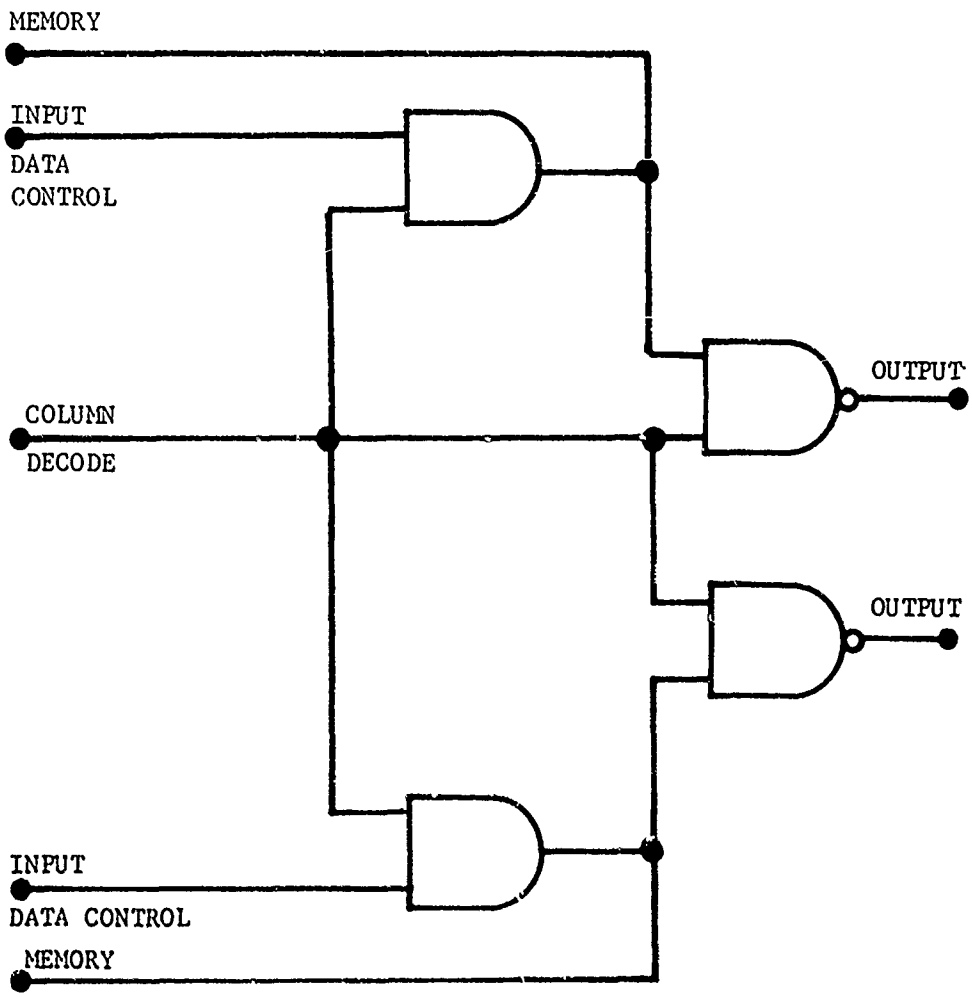


Figure 5-20 Logic Diagram, Sense Amplifier (Data I/O Control)

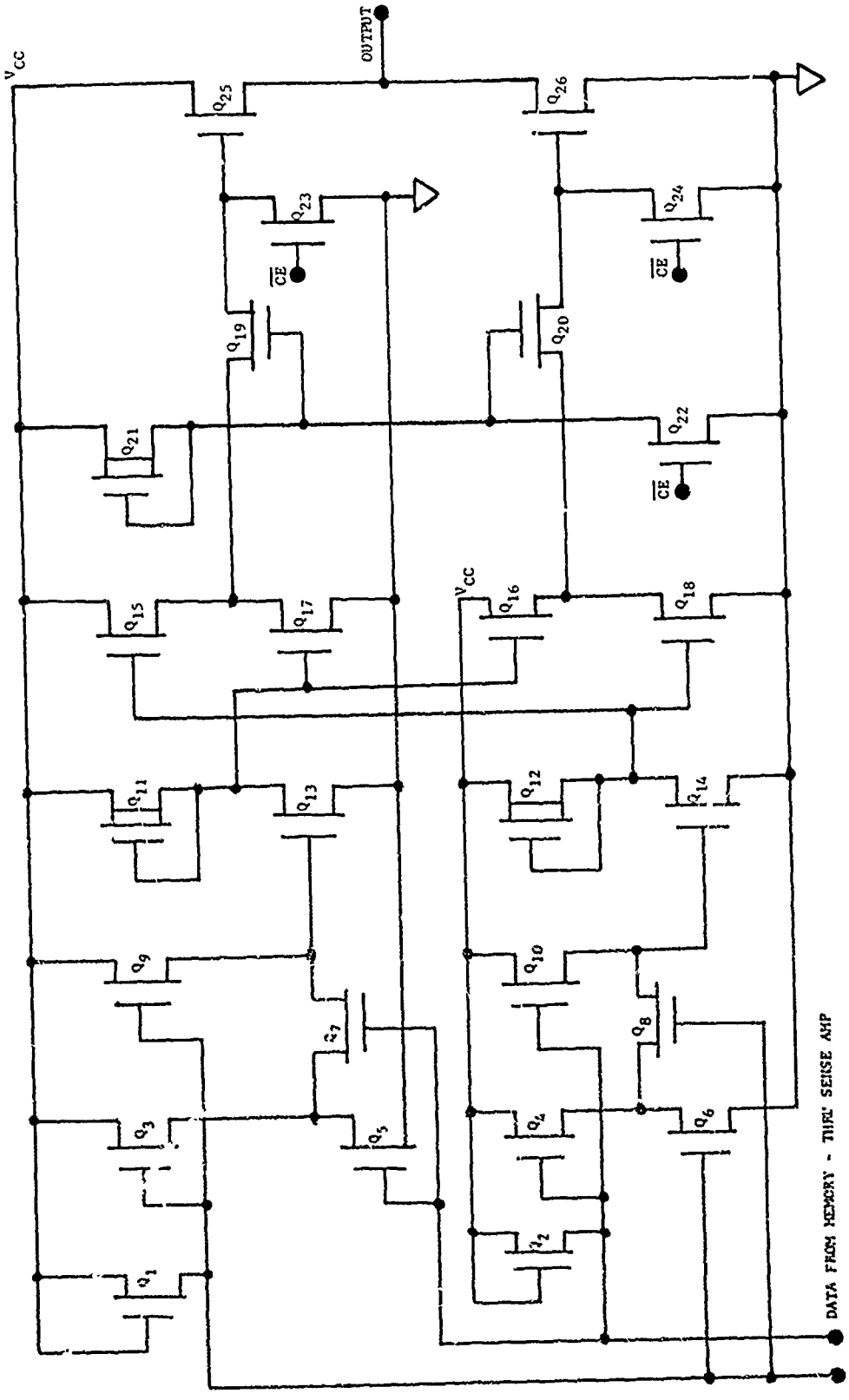


Figure 5-21 Schematic, Data Out Buffer

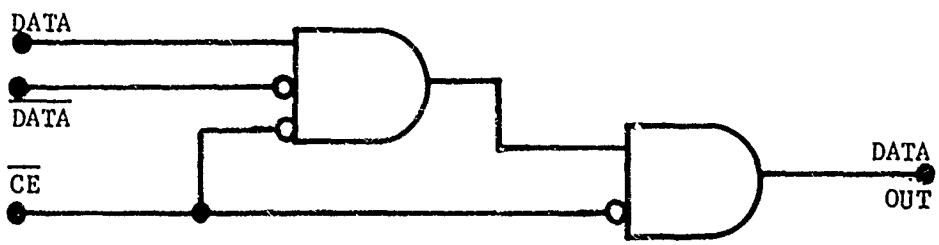


Figure 5-22 Logic Diagram, Data Out Buffer

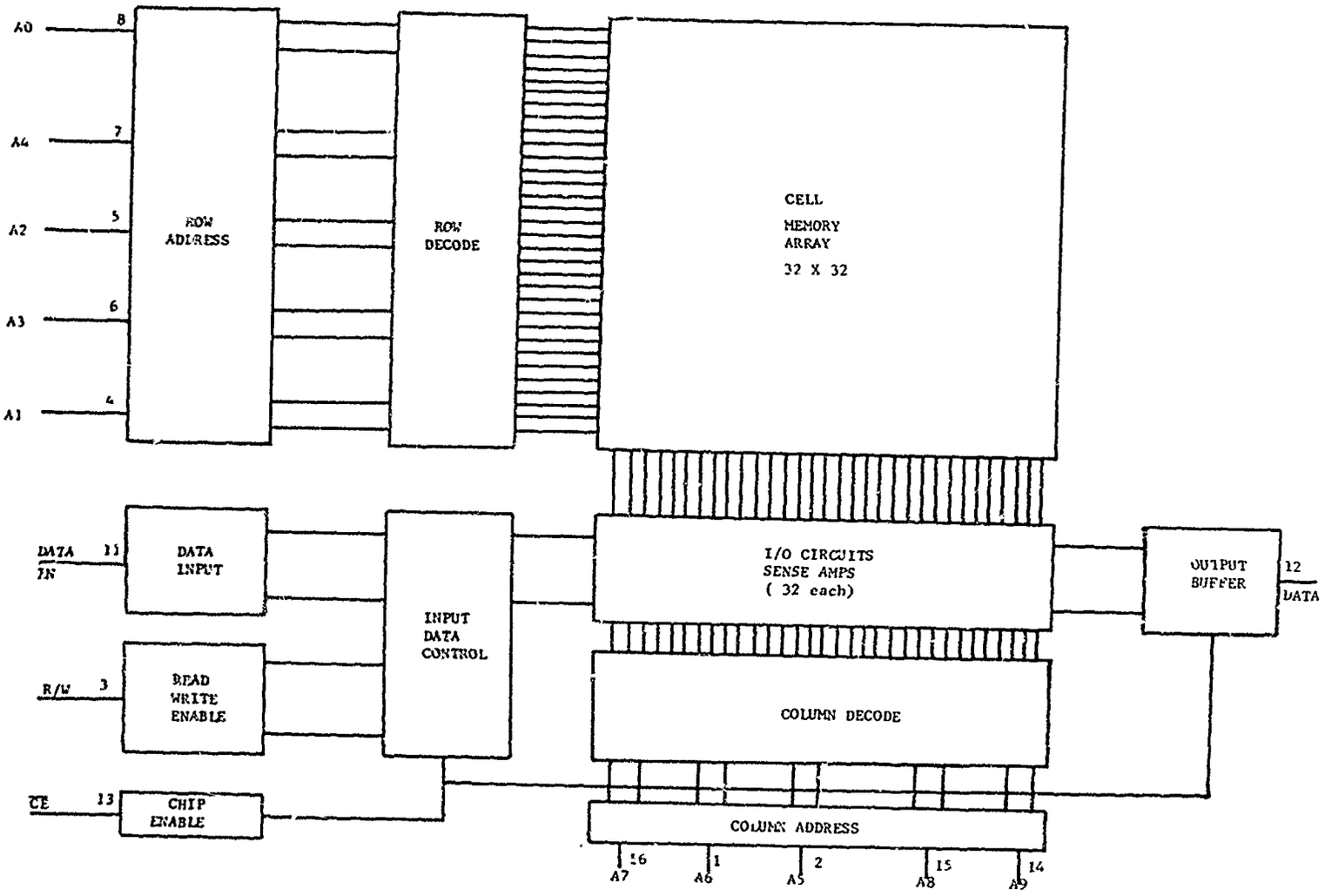


Figure 5-23 Block Diagram

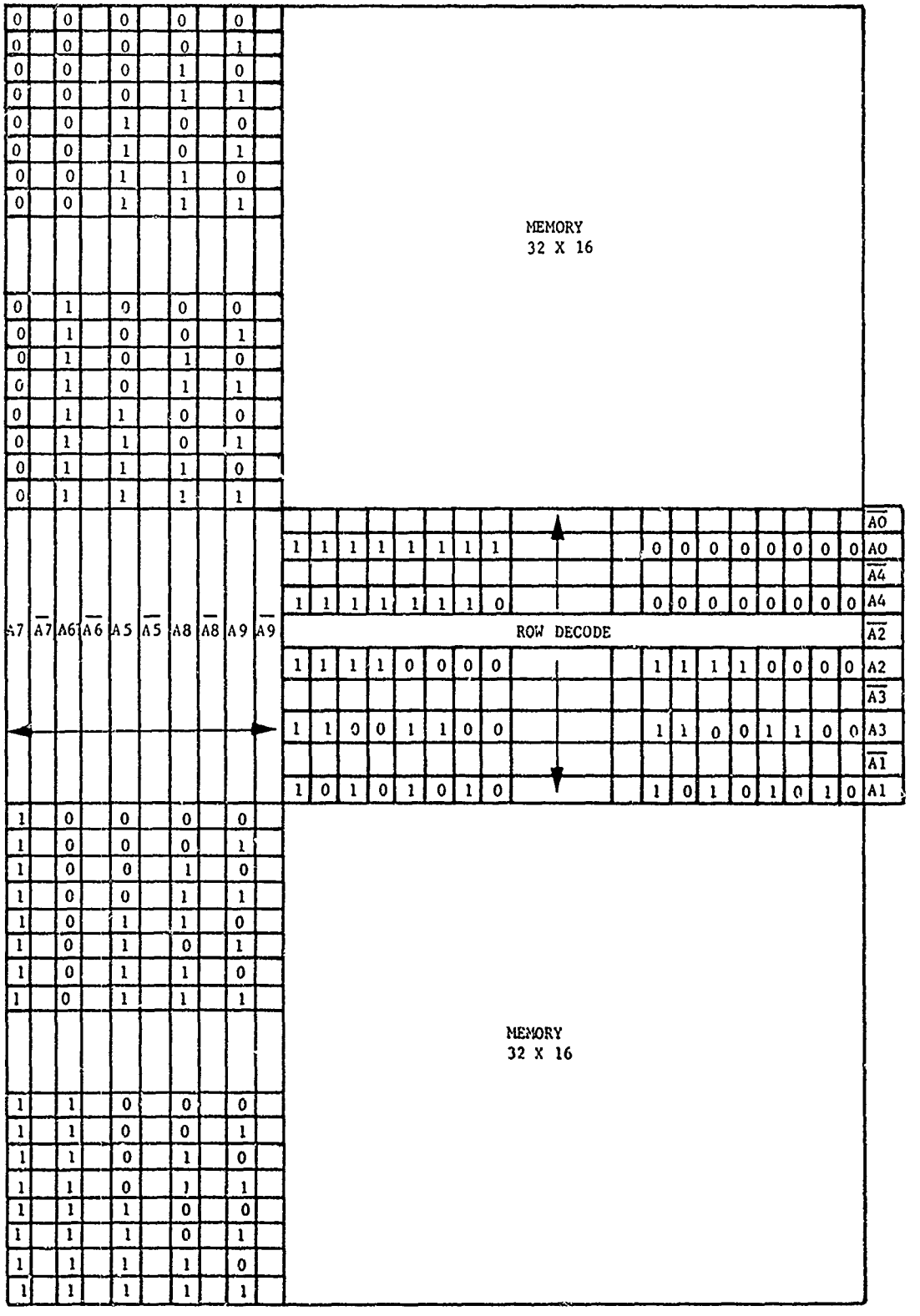


Figure 5-24 Bit Map

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4.6 4096 BIT DYNAMIC RAM (SiGATE NMOS)

Device Description

This device is a silicon gate N channel MOS dynamic 4096 x 1 bit RAM circuit. This version utilizes three supply voltages, -5, +5, and +12 volts. It is packaged in a 16 lead ceramic DIP. The device contains one chip select input and a three state output.

Electrical Characterization

Ten devices of this part type were used for this program. Five devices were used primarily for glass passivation removal and electrical test set-up verification, and five were electrically verified as meeting the parametric specifications.

The five good devices were electrically tested in accordance with the suppliers data sheet. These devices were serialized for individual identification. The DC parameters were measured, recorded, and are listed according to serial numbers in Table 6-I. All parameters were verified to meet the manufacturer's specifications.

During verification of the functional test curcuit, a problem developed which was isolated to the timing provided by the test circuit. Data could be written into and read out of memory, but errors kept occurring. These errors occurred for specific word locations, random word locations, and after a 30-60 second period of memory refresh. This indicated the input signal timing requirements were not being satisfied. A check of the timing signals identified two problems. In order to maintain the required signal conformation it was necessary to add line drivers to all ac stimulus lines from the functional test circuit. This modification improved the signal conformation but it was also necessary to decouple the dc power supply lines at the test socket for the memory device. Following these two functional test circuit modifications, the devices operated satisfactorily. An example of the waveform conformation obtained for this device is shown in Photo 6-1. This Photo shows the typical inputs for address, RAS, WE, and data input. The timing format is in four periods; buffer, refresh, buffer, read/-write and back to buffer. The refresh and read/write segments are identified in Photo 6-1. The double line on the address trace during the read/-write period results from the sequential cycling of addresses. The row and column addresses are multiplexed for this circuit. Therefore, row and column address states are determined during a 300 ns window located at the negative edge of RAS. In the example shown in Photo 6-1, the circuit is write enabled and is writing a high data state. The RAS refresh clock rate in this example is 125 kHz and the A0 row address refresh clock rate is 63 kHz.

The five parametrically tested devices were functionally tested using the memory test circuit. The functional test frequency (LSB) was 40 kHz and all five devices functioned properly. These five devices were used for all

characterization and failure analysis data collection and operational documentation.

Package Delid and Glass Passivation Removal

The ceramic package lid was removed by grinding using a 70 micron diamond impregnated wheel. When the lid was thinned to approximately 200 microns, a sharp probe was used to enter the cavity and break away the lid. Care was used to keep from contacting the interconnect wires or chip. The package cavity was flushed with a mild detergent/DI water solution; rinsed with DI water, followed by isopropyl alcohol and gently dried with dry nitrogen. This removed the ceramic particles which are introduced during delid.

Removal of the glass passivation was evaluated first using devices from the group of five evaluation devices. This device uses a single layer aluminum conductor which overlays a polysilicon layer. The polysilicon layer is used to provide gate elements and conductor interconnects. Both layers are overcoated with glass so it was necessary to remove about 1.5 microns of glass without significant damage to the conductors or circuitry. The etchant selected was a buffered HF etch. The etch used was:

280 ml ammonium fluoride	40%
35 ml hydrofluoric acid	48%

A great deal of difficulty was experienced in removing the passivation and maintaining functionality. Two problems were encountered. One is the same as was experienced on the previous silicon gate N channel devices. That is, removing sufficient glass to obtain dc voltage contrast; but not too much so that the circuit fails to function. The results from this evaluation indicated an optimum etch time of 4 to 5 minutes.

Device S/N 1 was etched for 4 minutes and the device remained functional. The device was examined on the light microscope. Based on the oxide coloring it appeared that additional glass should be removed. This device was etched for an additional 1 minute and it remained functional. Examination in the SEM at 1.2 kv showed very good voltage contrast. The problem encountered was that after 2 - 3 minutes of beam exposure, the circuit being examined ceased functioning. The electron beam was turned off and the circuit remained non-functional which verified the electron beam was not influencing circuit operation. This indicates the 1.2 Kev electrons have penetrated to the gate oxide and produced a trapped charge. This device was baked at 300^{o}C for 5 minutes to anneal the electron beam damage. Retest of the circuit showed it was functioning properly. It was again examined in the SEM a 1.2 kv; the same response was experienced. After 2 - 3 minutes of beam exposure the circuit failed to remain functional.

Device S/N 2 was prepared for SEM exam. This device was etched for 4 minutes and was verified to function properly. Examination by light microscope indicated additional etching was needed. This is based on the oxide colors observed across the die. If oxide colors are pastel or nonexsistent, then additional etching is performed. The previous etching experience provides a

reference basis for subsequent etching. A 5 minute etch on S/N 1 was too long; therefore, it was decided to etch S/N 2 for an additional 30 seconds. Following this additional etching the circuit remained functional. Examination of S/N 2 in the SEM at 1.2 kv produced the same results as S/N 1. After a short period of beam exposure the circuit stopped functioning.

Device S/N 3 was etched for 4 minutes. Testing showed this part was nonfunctional. Examination by light microscope showed metallization had been attacked and many stripes were lifted. This device had been packaged in Malaysia and S/N 1 and 2 were packaged in the Philipines. Even though the die geometries were the same, the die passivations were not comparable.

Device S/N 4 was etched for 2 minutes and tested. It remained functional. Light microscope examination indicated additional glass should be removed. This device was etched for another minute. Retest showed it was nonfunctional. Examination showed metallization had been etched open in localized areas. A photograph was taken to show the complete die and is provided in Photo 6-2.

Device S/N 6 was etched for 2 minutes and retested good. Light microscope examination showed additional glass should be removed. This time the device was etched for an additional 30 seconds. Following etching the device remained functional. Examination in the SEM at 1.2 kv beam voltage produced good voltage contrast and remained functional during examination. This device was used for voltage contrast documentation.

Removing the passivation can present one of the largest obstacles. This is due to the wide variation in glass characteristics. These variations exist from lot to lot for a single supplier. This makes it difficult to determine the point where further etching will effect circuit function.

Circuit Characterization

Device S/N 6 was placed in the SEM for circuit characterization. The SEM acceleration voltage used for this device was 1.2 kv. This voltage was selected to minimize electron beam damage in the circuit. No special preparation was used to reduce extraneous charging effects from the device package. Direct beam landings on nonconductive package surfaces were avoided to reduce charging on these surfaces. Also using a low acceleration voltage will reduce charging potentials on these nonconductive surfaces.

Operation of the complete chip was observed with all inputs active. For a chip of this complexity, observation of the overall circuit is probably more confusing than helpful in understanding its organization. In a circuit of this complexity there are too many circuit functions to comprehend by circuit observation. The address lines on this circuit are multiplexed to serve both row and column functions. The two six-bit addressed codes are latched in the circuit by two clocks, row address strobe (RAS), and column address strobe (CAS). The column address setup window, row address strobe leading edge to column address strobe leading edge minus the row address hold time, is 30 to 75 ns maximum depending on the device performance clas-

sification. Column address setup is the period allocated to change the 6 multiplexed address inputs from the desired row pattern to the desired column pattern. This constraint required modification of the functional test circuit to obtain proper functional performance.

As in previous circuit characterization the first circuit evaluated was a row address buffer. As circuit development progressed from the address input it was quickly realized that circuit definition was first required for the row address strobe and column address strobe circuits. Initially it was not apparent how many clock lines were developed by these circuits. Without knowing what timing relationships these clock lines had, it would be unlikely that operation of the row address buffer could be understood. Therefore, the first circuit evaluated was the row address strobe.

From the start the row address strobe provided the greatest challenge to this point in the study. The circuit involves such a large area of the die that it had to be documented on multiple photographs. Also the density of metal conductors combined with the length of some transistor silicon gates made it impractical to develop a circuit schematic from the usual voltage contrast and light photos.

It was apparent from the start that additional information was needed. What was needed was the ability to locate and determine the size of individual transistor cells. The density of the metal conductors obscured these cells so a third data format was developed. Device S/N 3 had experienced metal damage during glass passivation etching. This device was etched in a sodium hydroxide etch to remove all aluminum metallization. This device was used to provide photographs of the same areas documented by the voltage contrast and light microscope methods. The same basic procedure was used to develop the circuit schematic. Voltage contrast was used to locate the circuit which is actively responding to input signals. Without this visibility a great amount of time would be expended visually tracing through the circuitry. The voltage contrast also provides DC buss identification, relative signal phase for metal and silicon gate conductors and in some cases drain/-source diffusions. Note: This device utilizes three power supplies; +12, +5, and -5 volts. +5 volts is utilized only in the data output circuit. -5 volts is a V_{BB} source and does not appear on surface circuitry. Photo 6-3 is one of five voltage contrast micrographs used to document the row address strobe (RAS) circuit. These voltage contrast photos were taken with the RAS input cycling at 2 Hz, CAS high and CE low. Photo 6-4 is one of four light photographs. Photo 6-5 is a light photo example showing the circuit with the metallization removed. Because of the complexity of this device, and quantity of photographs needed to describe it, only two photographs of the circuit with metal removed will be included. Photo 6-5 shows the variation in transistor cell size with comparison of Q2, Q4, and Q5. Q2 has a total of 6 gate elements and is the input transistor. Also it is apparent in examining Photos 6-3 and 6-4, that identification of transistor cells and circuit interconnections are impractical using only these data. Another difficult problem presented by the RAS circuit is the random ordered circuitry. This is more typical of LSI interface logic and microprocessor circuitry. In these types of circuits repetitive cell organization is not very preva-

lent. Developing the schematic for this type of circuit requires the perseverance to construct the circuit cell by cell using all the available data. The RAS circuit provides basic timing references for a large part of the remaining circuitry. Other timing references are also provided by additional circuits which will be described later. No attempt was made to obtain an EBIC image from this circuit. Previous experience with silicon gate MOS showed it is not possible due to irradiation damage.

Using Photos 6-3, 6-4, and 6-5 a schematic for the RAS circuit was constructed (ref Fig. 6-1). The first timing pulse is generated at the drain of Q2; the translation from TTL to MOS levels is performed by transistor Q6 - Q9. The complete inverter consists of transistors Q2 through Q9 and capacitor C1. C1 is a bootstrap capacitor which produces a faster high response for the inverter and transistor Q1 is the input protection device. The clock generated by this inverter was designated clock A. This clock also interconnects with the gates of Q10 and Q18. This is the input to the second inverter circuit which includes Q10, 16 - 19, and C2. These devices are located by voltage contrast micrograph Photo 6-6 and light Photo 6-7. These photos are extensions to the upper right corner of 6-3 or right side of 6-4. In Photo 6-6 the voltage contrast responses are visible from many of the silicon gate conductors. This is made possible by removing a large part of the deposited glass passivation. The timing reference generated by this inverter was identified as clock B. This clock interconnects within the RAS circuit as well as with other circuit functions.

The B clock connects to the next inverter at the gate of transistor Q26. Also timing is provided from the clock-A inverter which connects with the gate of Q27. This inverter includes transistors Q25 - 34 and capacitor C4. These devices are located in Photos 6-3, 6-4, 6-6, and 6-7. The output provided by this inverter was identified as clock C.

A total of eight clock references (A through H) are developed by the RAS circuit. The propagation delay time from clock to clock is estimated to be 5 to 10 ns. Based upon this estimate the RAS input to clock H delay time would be 50 to 70 ns. The total RAS circuit is contained in voltage contrast and light Photos 6-3 to 6-12 and schematic Figure 6-1. The numbering sequence of the transistors is indicative of the order they were identified as the schematic was developed. The intermingling of transistors prohibited reconstruction of the circuit schematic in the same order that it operates. It is difficult to describe the bookkeeping procedure used in developing the schematic. Notations are made on the "working photographs" to maintain individual transistor cell identification, common circuit modes, and to keep track of what has been covered as you progress into the circuit. The notations consist of component numbers and different ink colors to uniquely identify circuit nodes, signal, supply and ground lines. A circuit of this type represents an unknown quantity. As the schematic evolves in its initial form it is unorganized and confusing. Therefore, it is most important that circuit interconnections be accurately conveyed from the photographs to the schematic form. When this is accomplished it can then be organized into a more understandable format. It is not very practical to expect to verify the schematic accuracy at this point. The schematic form now is very dif-

ferent from the chip layout and circuit tracing is more difficult. Individual circuit errors which become obvious during checking and operational verification of the schematic can be made. The point is, concentrate on accuracy during transformation of the circuit from the chip layout to the initial schematic.

As shown in the schematic the RAS circuit provides eight clock signals. This is simplified in Figure 6-2 which shows the Logic Diagram and Truth Table. The RAS circuit is basically a string of inverter circuits. The significance of this circuit will be better appreciated as other functional circuits are described and their dependence on these timing signals are shown.

The column address strobe (CAS) circuit was developed next. This circuit like RAS generates basic timing signals. The RAS signals being primarily related to row address functions and CAS to column address functions. The CAS circuit has much in common with RAS when it comes to developing a circuit schematic. This circuit is also comprised of a disarray of transistor cells and interconnections. The same procedure was used to develop the CAS schematic as was used for the RAS circuit.

Photo 6-13 is one of four voltage contrast micrographs of the CAS circuit. These photos were taken with the CAS input cycling at 2 Hz and CE low. Also gating signals are required from the RAS circuit. Therefore, a 125 ms positive going pulse was applied to the RAS input simultaneously with the positive cycle (250 ms) of the CAS input signal. This produced a low at the RAS input when the CAS input went low. It was obvious from voltage contrast observation that when RAS was high the CAS circuit was inhibited. The short pulse applied to RAS was used to eliminate confusion between the RAS and CAS signals.

The CAS input does not connect with the CAS circuit in the area shown in Photo 6-13. Photo 6-14 is the light photograph complement of Photo 6-13. This is one of three light photos of the CAS circuit. The CAS input connects with transistors Q2 and Q3 located in voltage contrast Photo 6-15 and light Photo 6-16. These photos are continuations of the upper right corner of Photo 6-13 or right end of Photo 6-14. Photos 6-17 and 6-19 are the remaining voltage contrast micrographs and Photo 6-18 is the remaining light photograph for the CAS circuit. The circuit schematic was developed using these photos and photos of this circuit without metallization. The schematic is shown in Figure 6-3. Again the component numbering sequence contained in the schematic depicts the evolution of reconstruction. The layout of this circuit complicated schematic development more than the RAS circuit. Even so it remains to be practical to trace the circuit and reconstruct it schematically.

The CAS circuit produces five clock signals which are referenced to the RAS and CAS input signals. These clocks were identified as clock J through clock N. The inverter circuit for clock J includes transistor Q2, Q4, Q23 - Q32, Q51, and Q52; and capacitor C3. Transistor Q1 is the input protection device. In addition to the CAS input signal, this inverter is gated by RAS

clocks C and D. If RAS is high these RAS clocks act to inhibit the CAS inverters. The component locations for the clock J inverter are shown in Photos 6-15 and 6-16. Transistors Q3, 28 and 29 perform the translation from the logic levels to 12 volt MOS logic levels. The CAS input signal interconnects with the gates of Q2 and Q3 and is also used to provide a data output inhibit. This function will be covered during the data output circuit description.

The clock J signal is used to generate the additional CAS clocks. The next clock sequence is identifed as clock K. This clock inverter includes transistors Q34, 35, 37, 38, and 39; and capacitor C4. The CAS inverter circuit design is very similar to that of the RAS inverters. The location of the clock K inverter components are shown in Photos 6-17 and 6-18. Very little voltage contrast signal response is visible for this inverter in Photo 6-17. The 12 volt V_{DD} buss obscures a major part of this circuit.

The clock K signal also generates clocks L, M, and N. These inverter circuits are shown in the schematic (Fig. 6-3) and the component locations are identified in Photos 6-13 through 6-19. The Logic Diagram and Truth Table for the CAS circuit is shown in Figure 6-4. The Truth Table shown is based on the condition that RAS is low. When RAS is low, clock C is high and clock D is low. If RAS is high, CAS is inhibited and all CAS clocks remain at the states shown for CAS high, regardless of the state of CAS.

The next circuit to be discribed is the row address buffer and latch circuit. This memory circuit is a 4096 x 1 bit which requires a total of 12 row and column address bits. This device multiplexes the address buss to reduce the number of package terminals dedicated to addressing. The address buss contains six address terminals which serve as both row and column address inputs. Through the use of timing signals, the address signals are applied to the row address buffer or the column address buffer.

The voltage contrast micrograph of the A0 row address buffer/latch circuit is shown in Photo 6-20. This photo was made with the A0 input cycling at 1.3 Hz, chip select low and RAS and CAS pulsed. A 70 ms pulse was applied to the RAS input and a 94 ms pulse was applied to the CAS input coincident with each transistion edge of the 1.3 Hz square wave applied to the A0 address buss. These RAS and CAS input pulses do not conform with the timing requirements of the device data sheet. However, they did provide the required stimulus necessary to obtain functional operation of the address buffer.

In Photo 6-20 the equally spaced black/white candy stripes visible at the A0 input and through the center of this photo is the 1.3 Hz address signal. The narrow white stripes visible on clock lines A and C is the pulse signal applied to RAS. Note that clock A is the complement of clock B. The sawtooth edges on the conductors are produced by an image shift which results from the 12 volt V_{DD} field changes. This effect was experienced on all of the memory circuits requiring 12 volt supply voltage. This field change occurs from dramatic changes in supply current distribution as the memory circuit responds to addressing. Photo 6-21 is the light photo of this buffer.

This circuit is also obscured by the metallization. Photo 6-22 shows this same circuit without the metallization. This exemplifies the need for all three data formats. The schematic for this circuit is shown in Figure 6-5.

A basic description of this circuit's operation follows. A row address word is applied to the six address lines of the address buss. The logic states on each address line are individually applied to the latch circuit (C1, Q5), through control of the transmission switch (Q1). The gate of Q1 is controlled by RAS clock B. Q30 is an input protection device. When RAS is high, clock B is high and Q1 is on. Also transistors Q4, Q7, Q14, Q27, and Q29 are turned off. These transistors isolate the latch circuit from the input and V_{SS}, or isolate the latch circuit from the buffer circuit. In addition, while RAS is high, transistors, Q2, Q3, Q6, Q8-13, Q16 - Q26, and Q28 are turned on. Note: With Q29 off V_{DD} is disconnected from the buffer circuit. This is primarily a precharge state that allows the circuit nodes in the latch circuitry to stabilize near the V_{DD} level.

When RAS is switched low, Q1 is turned off isolating C1 from the address buss and C1 stores the A0 logic state. RAS clock A goes high, B goes low, C goes high and D goes low. This turns on transistors Q4, Q7, Q14, Q27, and Q29; and turns off transistors Q6, Q8 - Q10, Q16 - Q18, Q22, and Q25. C2 and C3 act as bootstrap capacitors. When Q6 turns off and Q4 turns on, the inverse of the A0 logic level stored on C1 is applied to the node of Q2 source and Q3 drain. The TTL to MOS level translation is performed by transistors Q2 - Q5.

If a high level resides on C1, a low level will be applied to Q2/Q3. This causes Q18, Q19, and Q2 to turn off and Q10, Q11, and Q12 to remain on. This produces a stable state for the latch circuit. This state produces a high state at buffered output A0 and a low state at buffered output A0 - NOT.

If a low level resides on C1, a high level will be applied to the Q2 source. This causes Q10, Q11, and Q12 to turn off and Q18, Q19, and Q2 to remain on. This latch state produces a low state at buffered output A0 and a high state at buffered output A0-NOT.

The latch V_{SS} disconnect circuit (Q27 and Q28) and the buffer V_{DD} disconnect circuit (Q29) also service the remaining five row address buffer/-latch circuits. The A0 and A0-NOT buffer outputs are polysilicon conductors identified in Photo 6-22. Because these conductors are subsurface, it was difficult to obtain a voltage contrast response in Photo 6-20.

The logic diagram for this circuit is shown in Figure 6-6. The x-square on the input depicts the sample and hold circuit which is controlled by RAS clock B. The disable for the two NAND and two AND gates disable these gates when the disable line is low.

There are three other circuit functions of this device which use the same circuit configuration as that described for the row address latch/buffer. These circuits are the column address latch/buffer, data input latch/buffer, and chip select latch/buffer. These circuits are schematically identical;

however, in performing different functions, they are controlled by different timing references.

The column address A0 latch/buffer will be described next. The voltage contrast micrograph is shown in Photo 6-23. This photo was taken using the same signal inputs as used for the row address latch/buffer. The A0 input was cycling at 1.3 Hz, chip select was held low, and RAS and CAS inputs were pulsed in synchronization with the positive and negative slopes of the A0 signal. 70 ms pulses were appled to the RAS input and 94 ms pulses were applied to the CAS input. The column address latch/buffer circuits are independent of the row address latch/buffer circuits. Their inputs are the only points in common. Photo 6-24 is the light photograph of this circuit. The physical layout is very similar to the row address circuits.

The electrical schematic for this column address circuit is shown in Figure 6-7. This circuit is controlled by the time references of the CAS circuit. These references are CAS clocks J, K, L, and N. Circuit operation is the same as described for row address. The logic diagram is shown in Figure 6-8.

The addressing sequence for this device has stringent timing requirements. First, the row address code is applied to the address buss (A0 - A5). This must be accomplished prior to the negative transition of RAS. RAS and CAS are high during row address application. The negative transition of RAS latches the address code in the row address buffers. Following the negative transition of RAS, the column address code must be applied to the address buss (A0 - A5). This must be accomplished before the negative transition of CAS and within the RAS to CAS transition edge lead time (t_{RCL}). The window for this parameter t_{RCL} range from 30 to 55 ns depending upon the specified device speed. This window timing is the difference between row address hold time (t_{RAH}) and t_{RCL}.

The stringent timing requirements for dynamic circuits appear to preclude low frequency functional mapping; however, experience to present has shown that it is practical. Typically during functional mapping two memory locations are being addressed. During low frequency operation data are written into and read out of these two locations to verify functional circuit response. Some device types may not function correctly unless stringent timing requirements are met while other types are more tolerant. However, all the types evaluated to present have been found to function properly using low frequency addressing (this includes refresh). Alternatives are discussed in comparing stroboscopic voltage contrast, beam blanked functional mapping, and low frequency functional mapping in the general text.

The chip select latch/buffer circuit is similar to the row and column buffer circuits. The chip select circuit is located adjacent to the six column buffer circuits. It also uses the same CAS timing references used for controlling the column address buffers. The input is connected to the chip select terminal pin 13. Circuit operation is similar to that of the row and column address buffer circuits. Photo 6-25 is the voltage contrast micrograph for chip select. This photo appears to be a duplicate of Photo 6-23. The chip select input is being cycled at 1.3 Hz instead of the A0 input.

The circuit response is the same. The light photograph for chip select is Photo 6-26. Figure 6-9 is the schematic diagram. The chip select buffer provides two outputs, CS, and CS-not. The logic diagram is shown in Figure 6-10.

The last of the similar latch/buffer circuits is the data input buffer. The timing references for this circuit are received from the CAS and write enable circuits. The write enable circuit will be described later.

The data input circuit consists of two circuits. The first portion is the latch/buffer circuitry and the second portion is a latch/driver circuit. Photo 6-27 is the voltage contrast micrograph of the latch/buffer portion. This photo was taken with the data input cycling at 1.3 Hz, chip select was held low, and RAS, CAS, and write enable inputs were pulsed. 70 ms pulses were applied to RAS and WE inputs, and a 94 ms pulse was applied to the CAS input. The pulses were coincident with each positive and negative transition edge of the 1.3 Hz square wave applied to the data input. This results in writing alternating ones and zeros. Photo 6-28 is the voltage contrast micrograph showing the data input latch/driver circuitry. This circuitry is located to the right and above the data input buffer circuit shown in Photo 6-27. The micrograph of the second latch circuit was taken with 1.3 Hz applied to the data input, chip select low and RAS, CAS, and WE were pulsed. The pulse occurence was the same as for Photo 6-27. The pulse widths were 20 ms for RAS and WE, and 30 ms for CAS. The light photograph for the complete data input circuit is shown in Photo 6-8. The data input circuit schematic is shown in Figure 6-11. This schematic shows that the first latch is controlled by write enable generated clocks and the second latch is controlled by CAS generated clocks. The Truth Table for this circuit is included on the schematic. The data input signal is converted to two signals at the circuit output. One output Q is in phase with the input and output R is the complement of Q. This circuit is a duplication of the row address buffer/latch and operates in a similar manner. The logic diagram which describes this circuit function is shown in Figure 6-12.

The row decode circuit will be described next. A total of 64 decode circuits are used to decode the row addresses. The decode circuits are typically located alongside the memory array. In some cases they are located through the center of the memory array and split the array into equal halves. In either case they are easily recognized.

A dynamic circuit requires a greater number of prerequisites to enable operation of internal circuits. The identification of these requirements is generally straight forward. For this device the significance of the RAS and CAS clocks is better appreciated as more circuit functions are described. The address buffers could not function without proper clock timing. Therefore, the timing sequence dictated by the device data sheet must be followed to ensure proper functional operation of the device. It was not necessary to satisfy the timing speeds specified for this device in order to display circuit function. For example, to demonstrate the data input circuit operation it was necessary to provide the RAS negative transition prior to the CAS negative transition in order to enable the CAS circuit. However it was

not necessary that the CAS transition occur within the specified 50 to 100 ns of RAS. It would appear that this would also apply to other device types, but each would have to be evaluated individually. The key point is it was not necessary to satisfy timing speeds for displaying individual circuit operation. However they must be satisfied to obtain total circuit functionality.

The approach used for this study is to satisfy the timing sequence and minimize the circuit function. In low frequency functional mapping it is not possible to exercise the total circuit i.e., 4096 bits and maintain memory through refreshing. It is possible to alternate between two memory cells at low frequency and attain correct circuit function. In this device, the memory common to a given row is refreshed each time that row is addressed. Low frequency functional mapping provides a maximum refresh period of one second. This refresh period is generally acceptable for 25°C operation.

The row decode circuit was photographed with A0 cycling at 1.4 Hz, A1, A3, and A4 low, A2 and A5 high and RAS and CAS pulsed. 20 ms pulses were applied to RAS and CAS which were coincident with the A0 signal transitions. The voltage contrast micrograph for the row decode circuit is shown in Photo 6-30. In this photo, voltage levels are visible along the diffusion channels. The light photograph for row decode is shown in Photo 6-31. Both photos identify the address busses. The circuit schematic in Figure 6-13 was developed from these photos. In developing the schematic it is necessary to identify the related clock lines. This is accomplished by tracing these conductors back to the point of distribution. These points have been identified during earlier schematic development for these circuit functions. The clocks D, E, and G control the row decode circuit and are provided by the RAS circuit. Clocks D and E are in phase with the RAS input (pin 4) and clock G is out of phase.

The row decode circuit operates in the following manner. With RAS high V_{DD} is applied to the drains of the decode transistors through transistor Q1. All decode transistors have a low applied to their gates (Fig. 6-5 - transistors Q22 and Q25 are turned on). Q1 charges this circuit node including capacitor C1 to a potential near V_{DD}. Transistor Q9 is on and clock G (Q9 source) is low. Clock D is high and transistor Q12 is on. Transistor Q10 is on and Q11 is off and the memory row is not selected. When RAS goes low transistors Q1 and Q12 are turned off. If any one related address line is high the decode buss goes low, C1 is discharged, Q9 is turned off and this memory row is not selected. When all related address lines are high the decode buss remains charged high, C1 remains charged, Q9 is turned on, Clock G forces the memory row buss high (Q9 drain), Q11 turns on and forces Q10 gate low, and this memory row is selected. As the drain of Q9 is driven postitive by clock G, capacitor C1 acts to bootstrap Q9. The logic diagram for the row decode circuit is shown in Figure 6-14. The circuit is basically a six-input AND gate which is controlled by RAS clocks.

The row decode circuits control row access to the memory cells. Photo 6-32 is the voltage contrast micrograph of a typical memory cell being addressed. These memory rows are being enabled by the row decode busses which

run from the lower right to the upper left in Photo 6-32. This photo was taken with addresses A2 and A5 high, A1, A3, and A4 low with A0 cycling at 1.7 Hz, RAS and CAS were pulsed and chip select was low. 20 ms pulses were applied to RAS and CAS coincident with the A0 signal transitions. The memory columns are accessed by the column sense lines which are identified a and b and run from the lower left to upper right in Photo 6-32. The light photograph for typical memory cells is Photo 6-33. The row decode busses are polysilicon conductors and the column decode busses are aluminum conductors. The schematic of two typical memory cells is shown in Figure 6-15. Each memory cell contains two polysilicon capacitors and two row access transistors. An a buss and b buss interconnect the a terminals and b terminals shown on the photos and schematic. Two storage capacitors per memory cell provides complementary data storage for improved sense amplifier detection margins. The logic diagram for depicting a memory cell is contained in Figure 6-16. In addition to the decode functions the memory cells also interface with the refresh/precharge circuits. The refresh/precharge circuits will be described later.

Accessing a specific memory cell also requires column selection through the column decode circuit. Photo 6-34 shows the voltage contrast micrograph for the column decode circuit. The same address conditions were used to obtain this photo as were used for the row decode circuit. The RAS and CAS pulse widths were 100 ms and the address frequency used was 1.0 Hz. The A0 address lines are identified by the candy stripe pattern in Photo 6-34. The decode buss (common drains) response is visible and runs perpendicular to the column address lines. The light photograph 6-34 shows the decode circuit and locates all column address lines. The electrical schematic, Figure 6-17, shows the circuit is similar to the row decode circuit. The driver for the column decoder is contained in the sense amplifier. The logic diagram is a six input AND gate and is shown in Figure 6-18.

The column sense amplifiers are addressed through the column decode circuitry. There are 64 sense amplifiers and they are individually accessed through one of 64 six-bit column address words. Photo 6-36 is the voltage contrast micrograph for a column sense amplifier.

This photo was taken with addresses A2 and A5 high, A1, A3, and A4 low, A6 cycling and RAS and CAS inputs pulsing. A6 was cycling at 1.0 Hz and RAS and CAS were pulsed high for 20 ms at each A6 square wave transistion. The sense amplifier interconnects with the memory column busses located in the upper right corner of Photo 6-36. Memory cell b contains a high state and cell a contains a low state. The narrow dark stripes on the aluminum conductors are buss precharge potentials. Precharging will be discussed further in the following functional circuit section. The light photograph for the sense amplifier is Photo 6-37. Circuit density makes it difficult to locate the individual transistor cells. The schematic for this circuit is shown in Figure 6-19. This circuit performs a number of circuit functions. When RAS is high all nodes of Q6 - Q8 are driven to V_{DD} to precharge these busses. With RAS low and as each row is addressed the memory cells are refreshed. The low state cell (a or b) is refreshed through Q6 or Q7. For example if cell a contains a high state, Q6 turns on and a low state (clock

H) is applied to cell b of the addressed row. High state cell refresh is performed by another circuit and will be discussed later. Transistors Q2 and Q3 provide sense amp disable when RAS, CAS, or CS is high. The reading or writing of data in memory is conducted through Q4 and Q5. These transistors are controlled by Q1 (column decode input), Q2, and Q3. The Truth Table in Figure 6-19 outlines the basic circuit operations. The Logic Diagram for this circuit is shown in Figure 6-20.

The column precharge/refresh circuit is basically an extension of the sense amplifier. There are 64 of these circuits and they are located at the end opposite to the sense amplifiers and are interconnected by the column a and b busses. Photo 6-38 is the voltage contrast micrograph for this circuit. This photo was taken with A1, A3, and A4 low, A2 and A5 high, A0 cycling and pulsing RAS and CAS. A0 was cycling at 1.7 Hz. and RAS and CAS were pulsed high for 20 ms at each A0 square wave transition. The circuit interconnection with the column memory busses a and b is located in the lower left corner of Photo 6-38. Alternating ones and zeros were written into the cell common to this circuit to obtain candy striping on both circuit halves. The light photograph is shown in Photo 6-39. This photo shows five of the 64 circuits located along one side of the memory cell array. The schematic for this circuit is described in Figure 6-21.

Transistors Q1, Q2, Q7, and Q10 precharge capacitors C1, C2, and the busses a and b to V_{DD} whenever RAS is high. This provides an equal potential on the column memory busses at the time of memory cell access. This prevents an imbalance of the stored data at access due to unequal buss charges. When RAS is low, transistors Q3 - Q6, Q8, and Q9 restore the high level to the respective memory cell. For example, if the cell common to buss a contains a high or one state, Q3 turns on which discharges C1 and turns off Q9. Buss b is low so Q6 is OFF and Q4 and Q5 are on which applies V_{DD} to buss a. As described for the sense amp circuit it restores the low on zero state for the complementary side of the memory cell. The Logic Diagram for this circuit is shown in Figure 6-22.

The Q/R data buss is a key part of the operation for this device. The data input buffer and sense amplifier/refresh circuit interface with the Q/R data buss. The functional operation of these circuits have been described. To better understand the operational interface of the Q/R data buss, Figure 6-23 was prepared to show a simplified block diagram.

Data is entered onto the Q/R buss through the data input buffer. The write enable buffer controls the operation of the data input circuit. Write enable is dependent on timing clocks from RAS and CAS with the write enable address going low. Photo 6-40 is the voltage contrast micrograph for this circuit. This photo was taken with the write enable input cycling at 1.3 Hz and RAS and CAS pulsing positive for 70 ms and 94 ms respectively. RAS and CAS pulses were coincident with the positive and negative transitions of the write enable input. RAS clock C and CAS clocks J, K, L, M, and N provide the timing for the write enable circuit. The WE input is located at the lower left corner of Photo 6-40. RAS clock C can be followed from the clock

line subsurface to Q11 and then to C1 to Q10. Following a similar path in the light photograph, Photo 6-41, is more difficult.

The schematic for the write enable circuit is shown in Figure 6-24. Operation and control of this circuit is straight forward. A Truth Table is included with Figure 6-24 to help identify the operational modes. As shown in Figure 6-23 write enable provides three control signals; WE, WE-NOT, and P. All three connect with the data input buffer and P also connects with the sense amp latch. The Logic Diagram for write enable is shown in Figure 6-25.

Another primary control circuit related to the Q/R data buss is the sense amp control circuit. Sense amp control connects with the sense amp/refresh and data output circuits. Operation of the sense amp control circuit is determined by RAS, CAS, and CS. Photo 6-42 is the voltage contrast micrograph for this circuit. This photo was taken with CAS, write enable, and data-in at low levels; and RAS was cycling at 1.3 Hz. This circuit generates two control signals 0 and 0-NOT. The light photograph of this circuit is shown in Photo 6-43. Even in a relatively simple circuit like this, the metallization density obscures most of the transistor cells. The schematic of this circuit is detailed in Figure 6-26. A truth table is included which shows the major output states. This circuit generates two control signals 0 and 0-NOT. These signals control the sense amplifier and data output circuits. These two circuits are the only circuits which can be inhibited by chip select. When the chip is deselected, the 64 sense amplifiers and the data output circuit are inhibited. The Logic Diagram for the sense amp control circuit is shown in Figure 6-27.

The data output circuit transfers memory data from the data buss to the circuit output terminal. This circuit also generates clock S which acts to control the data buss latch circuit. Photo 6-44 is the voltage contrast micrograph for the output circuit. This photo was taken with addresses A1 - A3 high, A4, and A5 low, A0 cycling at 1.3 Hz, and RAS and CAS being pulsed high. The RAS and CAS inputs were pulsed high for 20 ms coincident with the A0 input signal transitions. The output transistors for this circuit are Q56 and Q57 located in the bottom center of Photo 6-44. Closer examination of these two transistors show the drain of Q56 is at V_{CC} (5 volts) and the source of Q57 is at V_{SS}. The output terminal is connected with the interdigitated metal stripe which is located between Q56 and Q57. The candy stripe pattern located on this metal stripe was produced by the one and zero data being read out of memory. The light photograph for this circuit consists of three Photos; 6- 45, 46, and 47. The clock and control lines are identifed on these photos. Figure 6-28 shows the schematic circuit for the data output stage. The circuit in the lower left portion of this schematic generates clock S. This clock controls the data output latch and sense amp latch circuits. To enable these latches, RAS, CAS, and CS inputs must be low. The data output latch circuit is similar to other latches used in this device. With CAS high, capacitors C1, C2, and C3 are charged to V_{DD}. When CAS switches low, clock M goes low and clock L goes high. This holds Q5 and Q6 on to acquire data from the Q/R data buss. A short time after CAS switches low with RAS and CS low, clock S switches high disconnecting the latch inputs from the Q/R data buss and setting the latch. The latch data

is applied to the output stage. A high Q level produces a high state on the output. The output data remains valid after CAS switches high. CAS clock L goes low and disconnects the latch circuit from the output at Q28 and Q29. This allows the applied data to reside as a charge on the output transistor gates. The device specification shows the minimum data storage time for the output is 32 ms. A Truth Table is included in Figure 6-28 to describe the basic operation of this circuit. The Logic Diagram for this circuit is shown in Figure 6-29.

The final circuit to be described for this circuit is the sense amp latch. As shown in Figure 6-23 this circuit connects with the Q/R data buss; and operation is controlled by clock M from CAS, clock P generated by write enable, and clock S generated by the data output circuit. The voltage contrast micrograph for this circuit is shown in Photo 6-48. This photograph was taken with write enable cycling at 1.3 Hz, RAS and CAS being pulsed, and row and column addresses, and data input low. RAS and CAS were pulsed high for 25 ms at each transition of the write enable input. The light photograph for this circuit is shown in Photo 6-49. The schematic for the sense amp latch is illustrated in Figure 6-30. This latch circuit is similar to others used in this device. The circuit is enabled by CAS switching from a high to a low state. This accesses the circuit and latches the Q/R buss data. The circuit is inhibited when write enable is low and the Q/R latch inputs exhibit a high impedance. This latch circuit provides temporary storage for sense amp data. The only driver circuit on this buss is the data in buss driver. This driver is the only circuit which is capable of driving the sense amplifier and writing data into memory. The sense amp latch temporarily stores data outputted by the sense amplifier. A Truth Table is included in Figure 6-30 to identify basic circuit operation. The logic diagram for the sense amp latch circuit is shown in Figure 6-31.

As stated earlier the Q/R data buss represents the heart of this memory circuit. All memory data transactions are handled by this buss. This device provides three functional operations; read, write, and read-modify-write. Basically the read operation occurs when write enable is held high. The write operation occurs when write enable is switched low prior to CAS. The data-in level is written into memory and the data-out latch will contain the data written into memory. The read-modify-write operation occurs when write enable is switched low after CAS goes low. In this mode the data output latch will contain the data read from the memory cell prior to writing in new data. Another important factor is related to chip select. When the chip is deselected only two functional circuits are inhibited, the sense amplifiers and data output. Therefore when memory devices are operated in parallel, all RAS, CAS, row address, row decode, column address, column decode, refresh, data-in and write enable circuits are active.

The chip organization is shown in Photo 6-50. A block diagram is shown in Figure 6-32. These two references provide a good overview of the functional organization and die layout for this device. There are four additional circuit functions identified in the chip organization and block diagram which were not shown on the data sheet block diagram. These functions were refresh, precharge, sense amp control, and sense amp latch. The die dimen-

sions are 130 mils x 160 mils. The bit map for this device is shown in Figure 6-33. Developing the bit map for this device was straight forward. The active row and column lines were easily identified by voltage contrast. The address code to addressed row and column location is identifed visually by real time observation of circuit operation during low frequency and manual switch addressing. This information is simply conveyed through the bit map.

Failure Analysis

Failure analysis of this circuit was demonstrated using two devices. Both devices were functionally tested and verified to be operating correctly. They were decapped and the glass passivation was removed using the same procedure described for the device used during circuit characterization. The devices were retested to verify functional operation. The same procedure was used for this device as for the previous devices. The failures were introduced and the isolation was made by different people. The failed devices were given to the person making the isolation without any details regarding the failure introduced. This was done to provide the best test in evaluating the practicality of failure isolation. In retrospect the greatest challenge was placed on the person generating the failure to provide a difficult problem for isolation. For the failures generated, the isolation for the most part was routine. One key factor relative to this experience is the detailed knowledge of the circuits design and chip organization which was obtained during circuit characterization. This intimate familiarity was invaluable in evaluating the circuit response during functional testing, applying this information to determine what area of the circuit was malfunctioning and, where this portion of the circuit is physically located on the die. Without this knowlege the success ratio for failure isolation would be dramatically reduced.

A second key factor is that this intimate familiarity can be realized through device characterization. This knowledge can be obtained on a practical basis.

The first device used for failure isolation was identified as S/N 9. A failure was introduced and the device was analyzed by another person. Functional testing showed that all lows (zeros) could be written into memory but all highs (ones) could not. Further evaluation showed that a high could not be written into memory whenever row address A0 was addressed low. This shows the failure to be related to row address A0.

The circuit was placed in the SEM and the A0 row address buffer/latch circuit was examined. The A0 input was cycling at 1.3 Hz, RAS and CAS were pulsed high and the remaining row and column addresses were held low. The RAS and CAS inputs were pulsed high for 2 ms and these pulses were coincident with the A0 input signal transitions. It was determined that A0 row address buffer and latch were operating. It was also noted that an output was present for A0, but no output was present for A0-NOT. Reference the voltage contrast micrograph, Photo 6-51, of A0 row address buffer/latch circuit. The arrow at A0 locates this output response. The arrow at A0-NOT shows no output response. This photo can be compared to Photo 6-20. Trac-

ing back into the circuit from the A0-NOT output, it was noted that the metal stripe common to the gate of Q20 was not changing (double arrow in Photo 6-51). Further examination and comparison with Photo 6-20 showed there was an OPEN in this metal stripe. This was the failure that was intentionally generated in this circuit. The metal had been scribed open.

The second device used for failure isolation was identified as S/N 10. A failure was introduced and the device was given to another person for analysis. Functional testing showed proper operation when all ones or all zeros were written into memory. When an arbitrary word location was selected and complementary data was written into this single location, the data state written last was always the data state read out for all other word locations addressed. It gave the indication that the last data state written into memory was hanging up in the circuit and was read out for all subsequent addresses. From these symptons the problem appeared to be related to the Q/R data buss.

The circuit was placed in the SEM and examined using voltage contrast. All row and column address lines were cycled sequentially (LSB = 1.3 Hz), and RAS and CAS were pulsed high for 2 ms at each address signal transition. The row decode and memory access sequence was checked and found to be operating properly. The column decode sequence was examined and it was also operating properly. During examination of the memory access through the sense amplifiers, it was noted that there was no access through sense amplifiers 63 (column address code 111110) and 64 (column address code 111111). Further examination indicated no column decode enable was being supplied to these two sense amplifiers. These two decode circuits were examined while cycling A0 at 1.3 Hz, pulsing RAS and CAS at 2 ms and forcing A1 - A5 high. Photo 6-52 shows the voltage contrast micrograph obtained at this time. Address A1 was switched low and Photo 6-53 was taken. In Photo 6-53 the column enable signals are visible for columns 61 and 62. The column enable signals for column 63 and 64 were not visible in Photo 6-52, Further examination of this area showed that the V_{SS} connection for column decode circuits 63 and 64 had been scribed open (ref arrow in Photo 6-52). This results in columns 63 and 64 being accessed all the time. This dc high state could not be detected by voltage contrast and therefore, it appeared these two columns were not being accessed. This also agrees with the unusual responses from the memory. The last data written into memory was also written into the cells common to column 63 and 64. When the memory was read the logic states located in these two columns were apparently dominate over the single cell containing complementary data. The important point to realize in this example is that the area of the failure site was successfully located. This was the primary purpose of this exercise.

A second failure was introduced into device S/N 10. Functional testing showed that highs cannot be written into any cells of column 1. The cells common to column 2 were functional. Testing was limited by the presence of the first failure. The second failure was isolated to column 1 by functional testing.

This circuit was examined in the SEM using voltage contrast. The A0 address was cycled at 1.3 Hz, RAS and CAS were pulsed high for 2 ms at each A0 transition, and A1 through A5 were forced low. The column decode circuits for address 000000 and 000001 were examined. This showed that column decode circuit 1 was not functioning and circuit 2 was operating properly (ref Photo 6-54). Circuit 1 was examined closely to locate the cause of circuit failure. It was not possible to identify a physical or electrical cause for decode malfunction. Based on the functional test response for this failure and comparison to the symptons of the first failure isolated in this device; it appears that in this second malfunction, the memory cells common to column 1 cannot be accessed. This indicates that the decode line for column 1 does not go high. Reviewing the schematic in Figure 6-17 shows that one of the decode transistors has excessive leakage or a leakage path is present between the decode line and V_{SS}. Locating the leakage path would normally require mechanical probing and circuit isolation. In this instance, the failure was introduced by exposing transistor Q7 to a 5 kv beam for 2 minutes. This irradiation caused transistor Q7 to stay on regardless of applied gate voltage.

The characterization and study of this circuit type presented a multitude of challenges which began with attempts to successfully remove the glass passivation. SEM voltage contrast examination successfully met the challenge of providing operational circuit responses for complex dynamic memories. These data provide an invaluable resource for identifying and understanding functional circuit operation. Furthermore, the voltage contrast data provides the necessary compatability for verifying the accuracy of the developed schematic to actual circuit operation.

This is readily accomplished when multiphase data is present on a single micrograph.

TABLE 6-I DC PARAMETERS

S/N 1	7720	S/N 8	7729	V_{DD} = 12 volts
S/N 2	7721	S/N 9	7730	V_{CC} = 5 volts
S/N 3	7725	S/N 10	7731	V_{BB} = 5 volts
S/N 4-7	7727			

S/N 1	2	3	4	5	6	7	8	9	10	V_{IN} = 7.0V PIN	PARAMETERS
0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	2	I_{LI}
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	3	
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	4	
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	5	
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	6	
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	7	
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	10	
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	11	
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	12	
0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	13	
0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	15	I_{LI}
										I_{LI} Max = 10uA	
										Volts 5.5V	
0.0uA	0.0uA	19.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	14	I_{LO}
										I_{LO} Max = 10uA	

TABLE 6-1 (concl)

S/N 1	2	3	4	5	6	7	8	9	10	V_{DD} = 13.2V PIN PARAMETERS
0.52mA	0.67mA	0.67mA	0.66mA	0.82mA	0.68mA	0.60mA	0.78mA	0.71mA	0.76mA	8 I_{DD_1}
										I_{DD} Max = 2mA
0.4uA	1.3uA	0.4uA	0.7uA	4.5uA	0.8uA	0.2uA	2.6uA	0.6uA	0.9uA	1 I_{BB_1}
										I_{BB} Max - 50mA
0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	0.0uA	9 I_{CC_1}
										I_{CC} Max = 10mA
										V_{DD} = 12.0V
3.67mA	4.25mA	4.18mA	4.08mA	4.85mA	4.14mA	3.85mA	4.71mA	4.24mA	4.41mA	8 I_{DD_2}
										I_{DD} Max - 30mA
5.1uA	6.7uA	5.1uA	8.3uA	10.6uA	7.1uA	2.5uA	8.0uA	7.5uA	5.3uA	1 I_{BB_3}
										I_{BB} Max - 325mA
.138mA	.138mA	.138mA	.138mA	.138mA	.138mA	.138mA	.138mA	.138mA	.138mA	9 I_{CC_2}

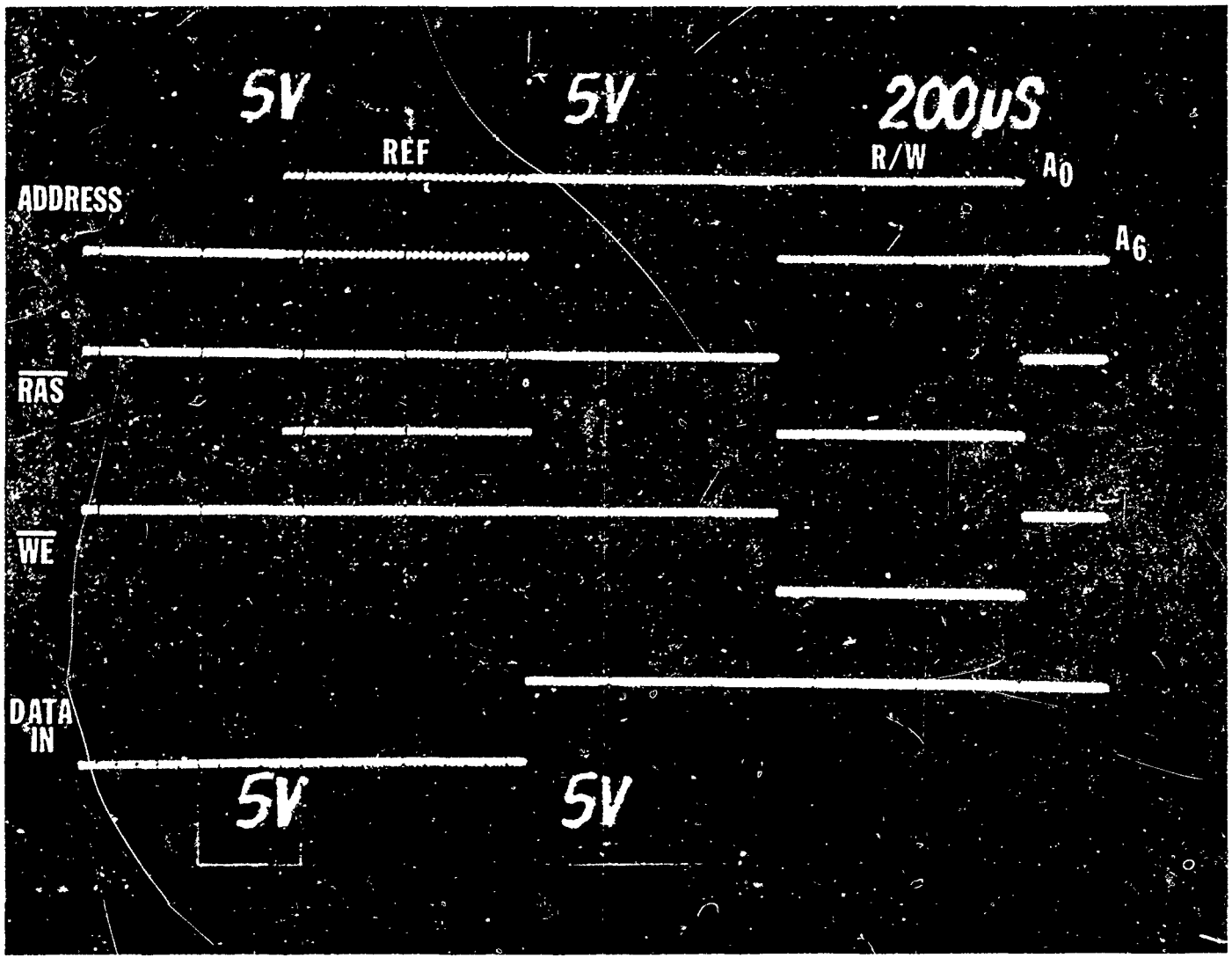

Photo 6-1 This Photograph Shows the Typical Signals for Four of the Circuit Inputs.

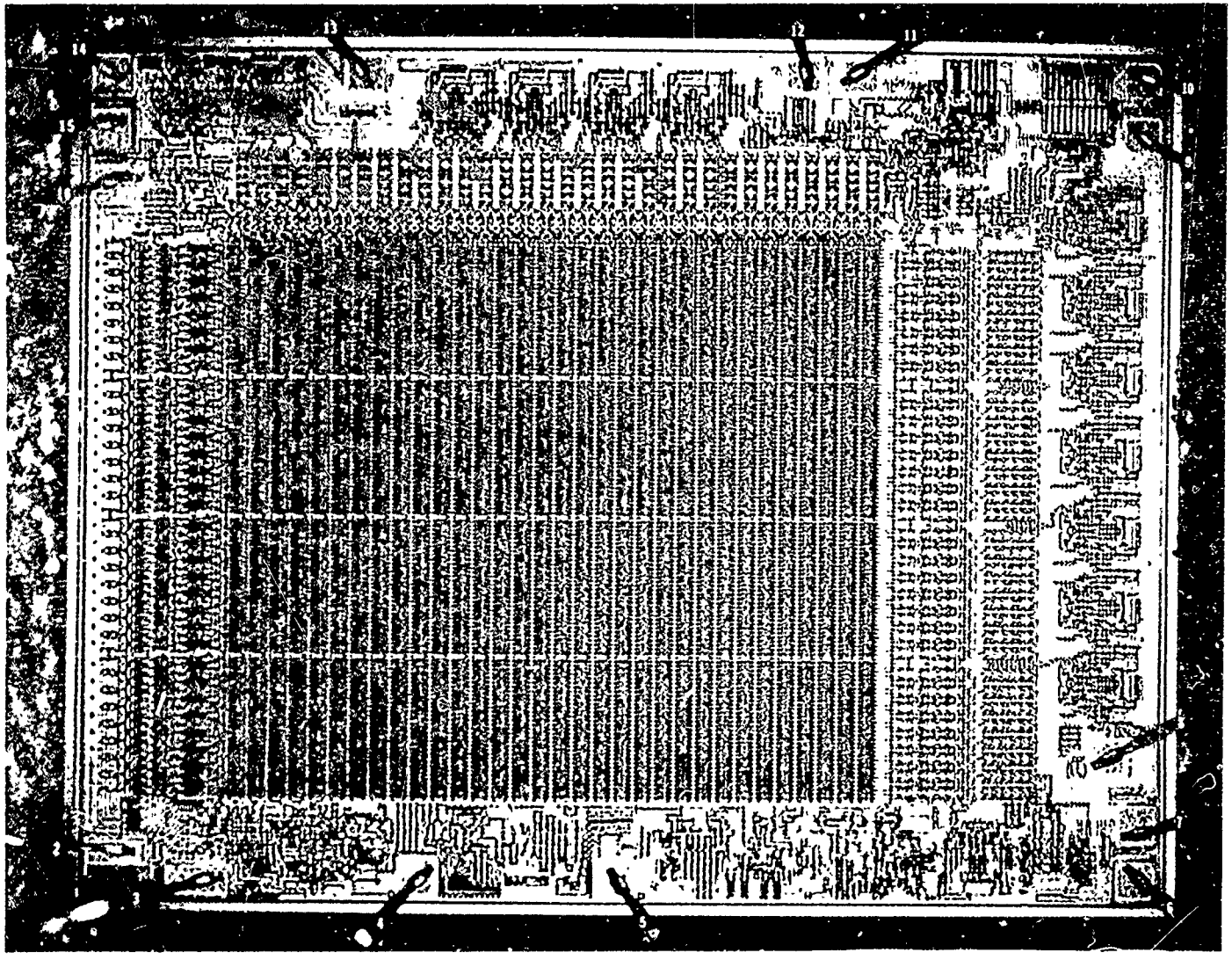

Photo 6-2 Photograph of the Complete Die. Mag. - 40X

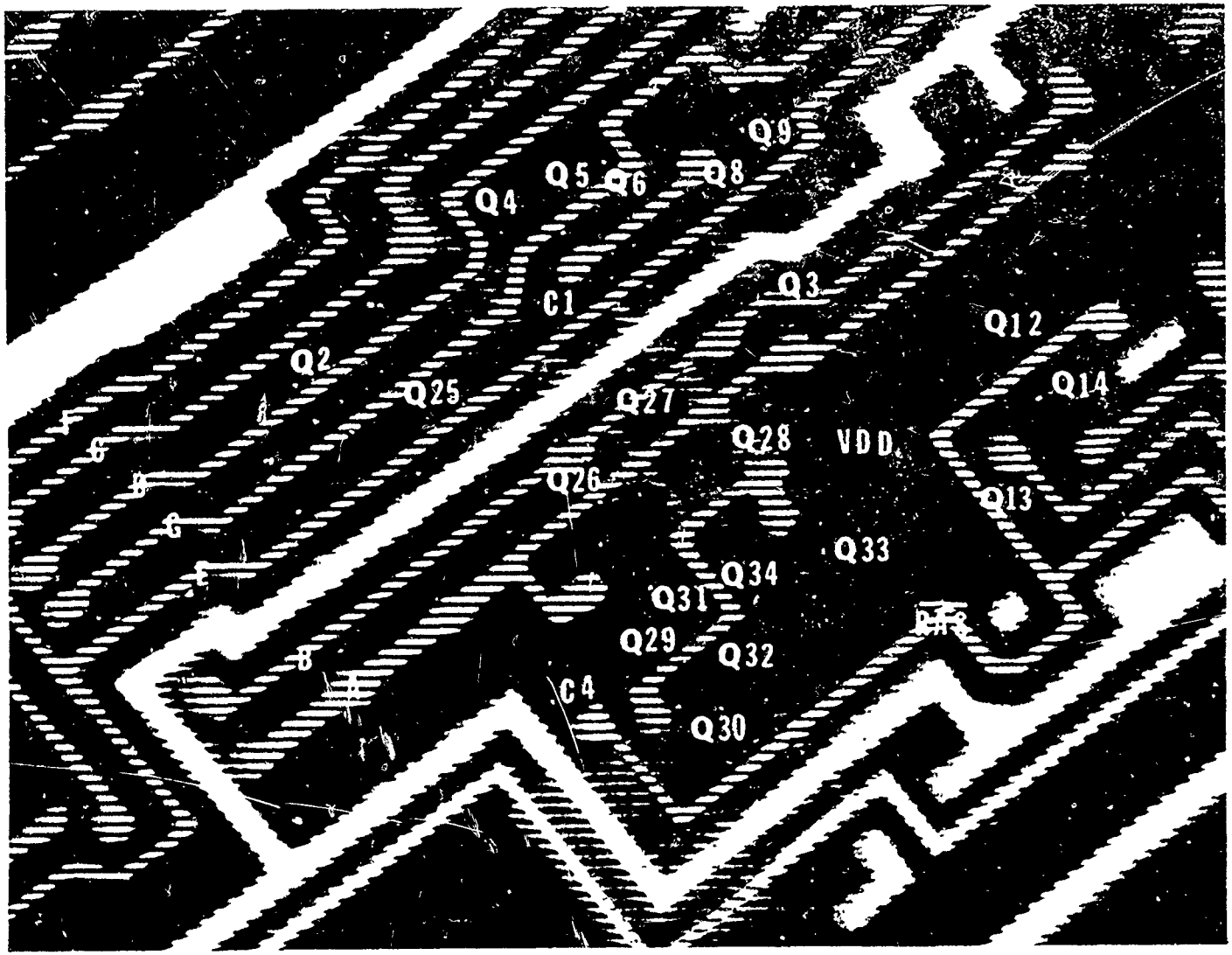

Photo 6-3 One of Five Voltage Contrast Micrographs of the Row Address Strobe (RAS) Circuit. 1.3 KV, Mag. - 500X

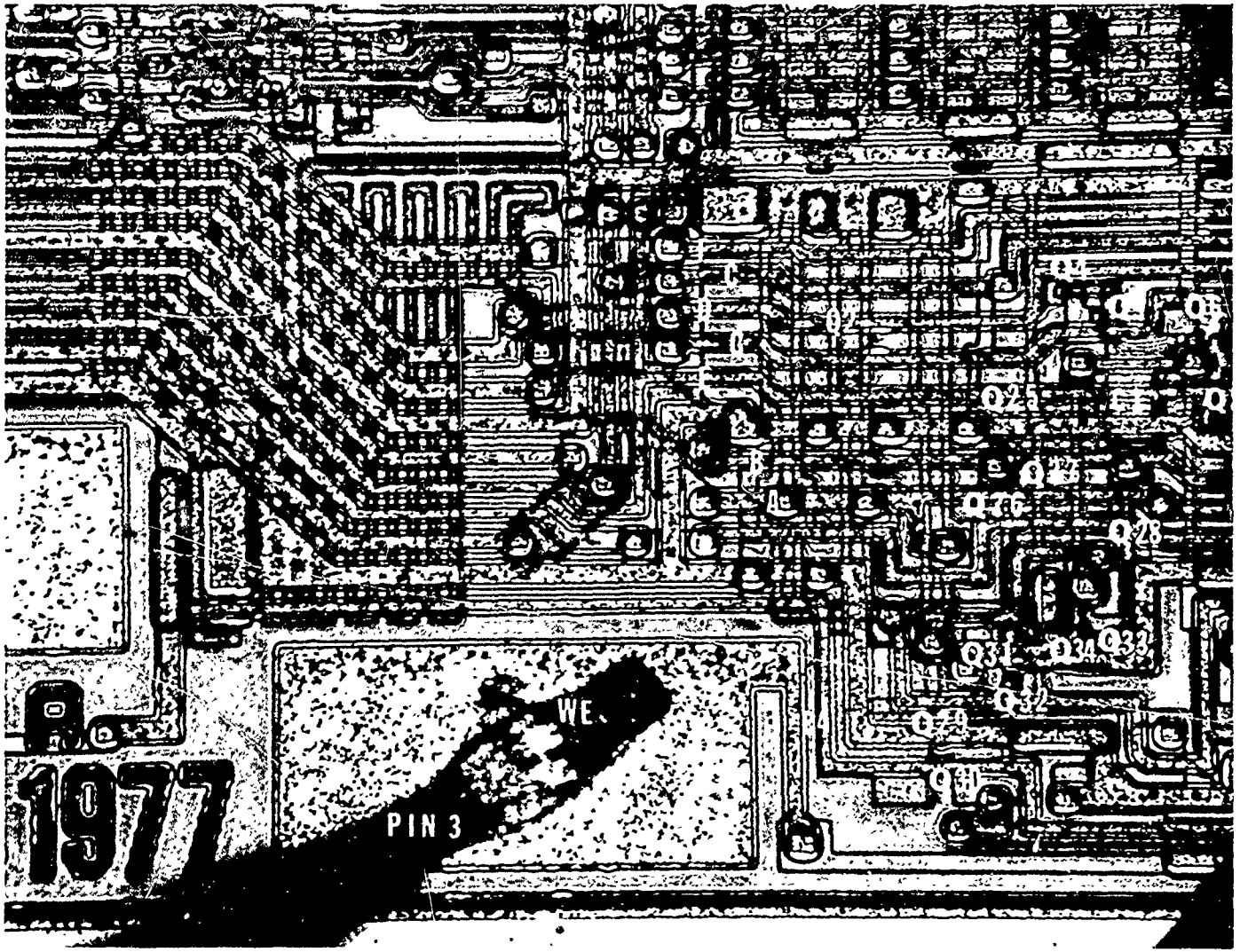

Photo 6-4 One of Four Light Photographs of the RAS Circuit. Mag. - 300X

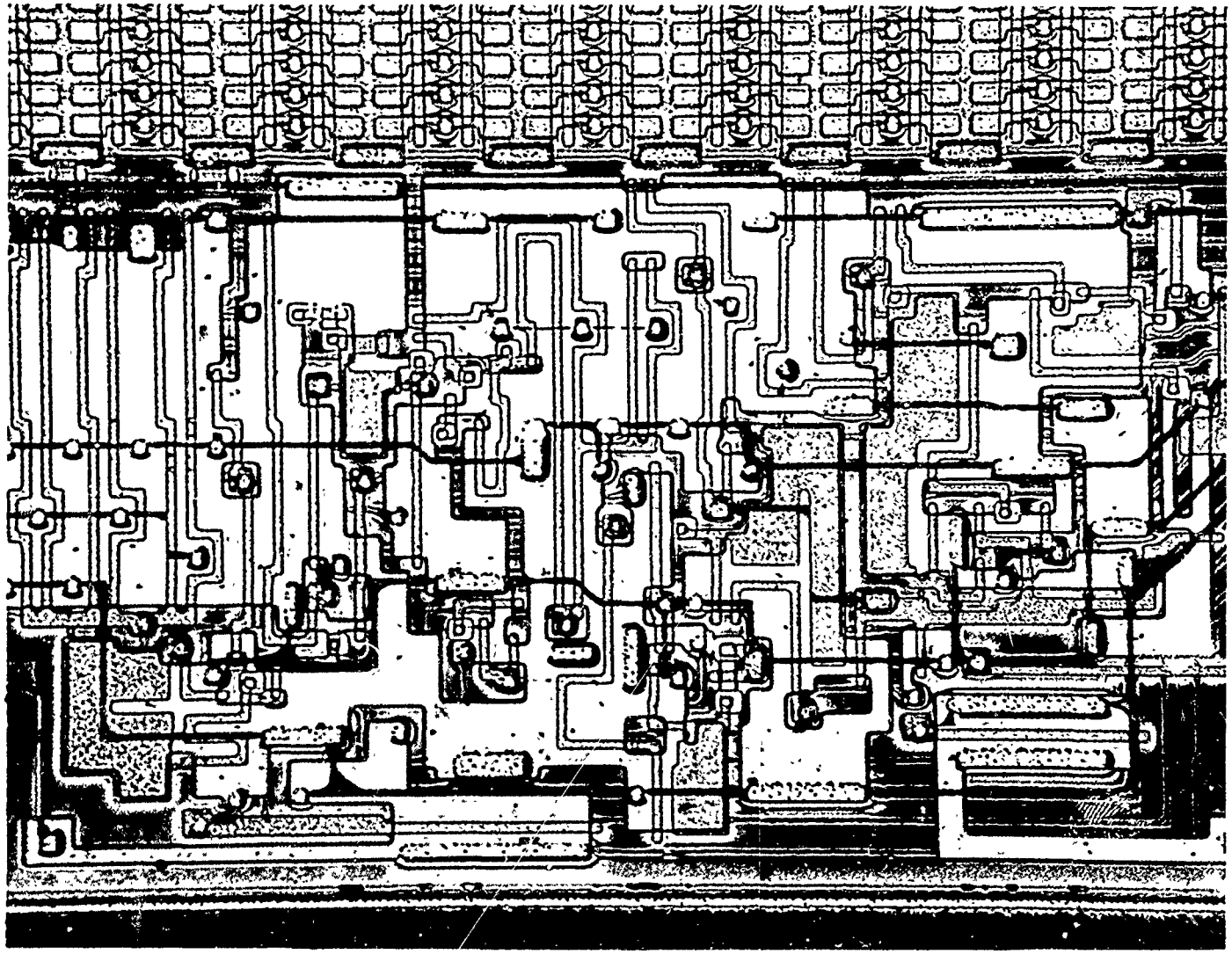

Photo 6-5 Light Photograph of a Portion of the RAS Circuit with the Metallization Removed. Mag. - 300X

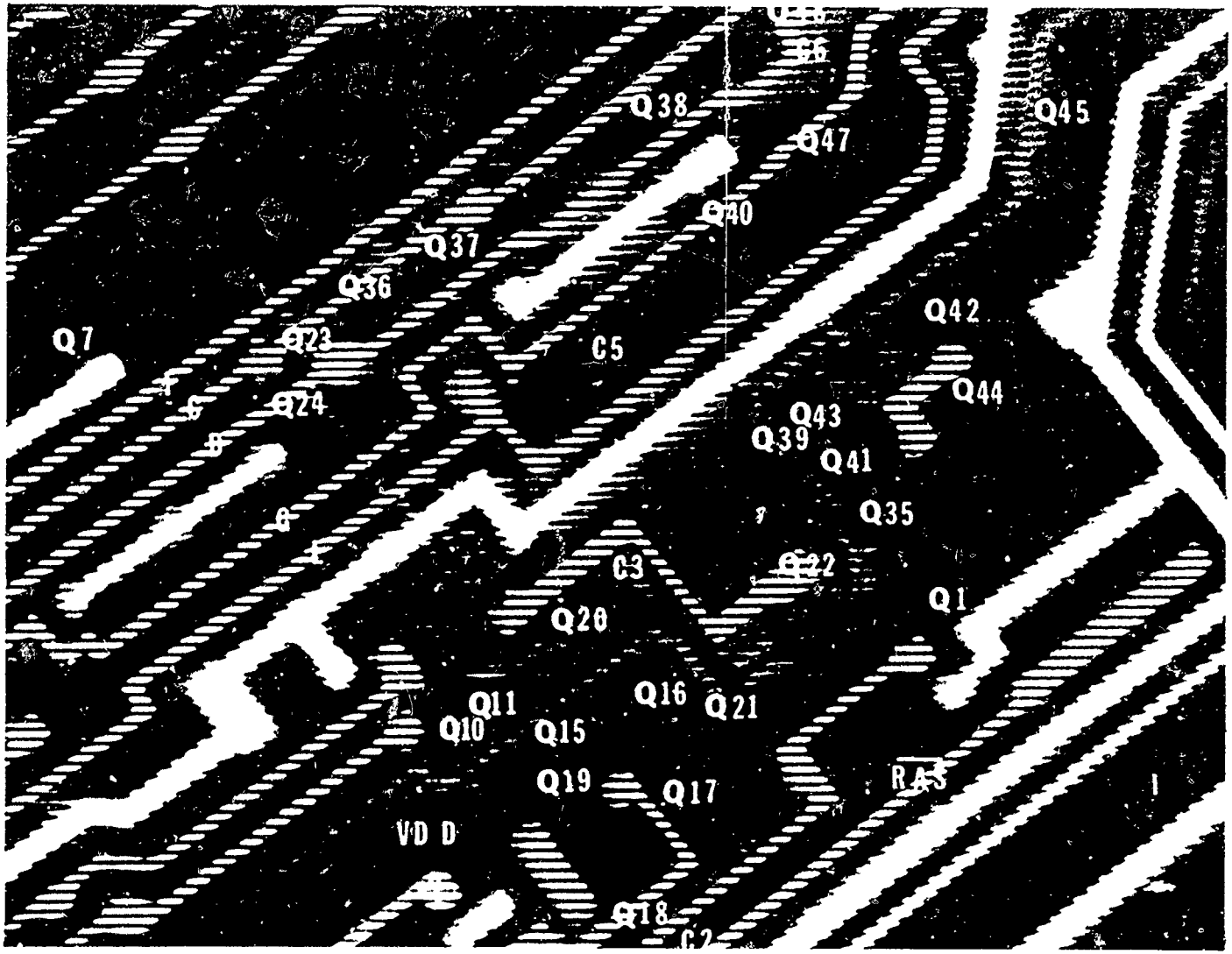

Photo 6-6 Two of Five Voltage Contrast Micrographs of RAS Circuit. 1.3 KV, Mag. - 500X

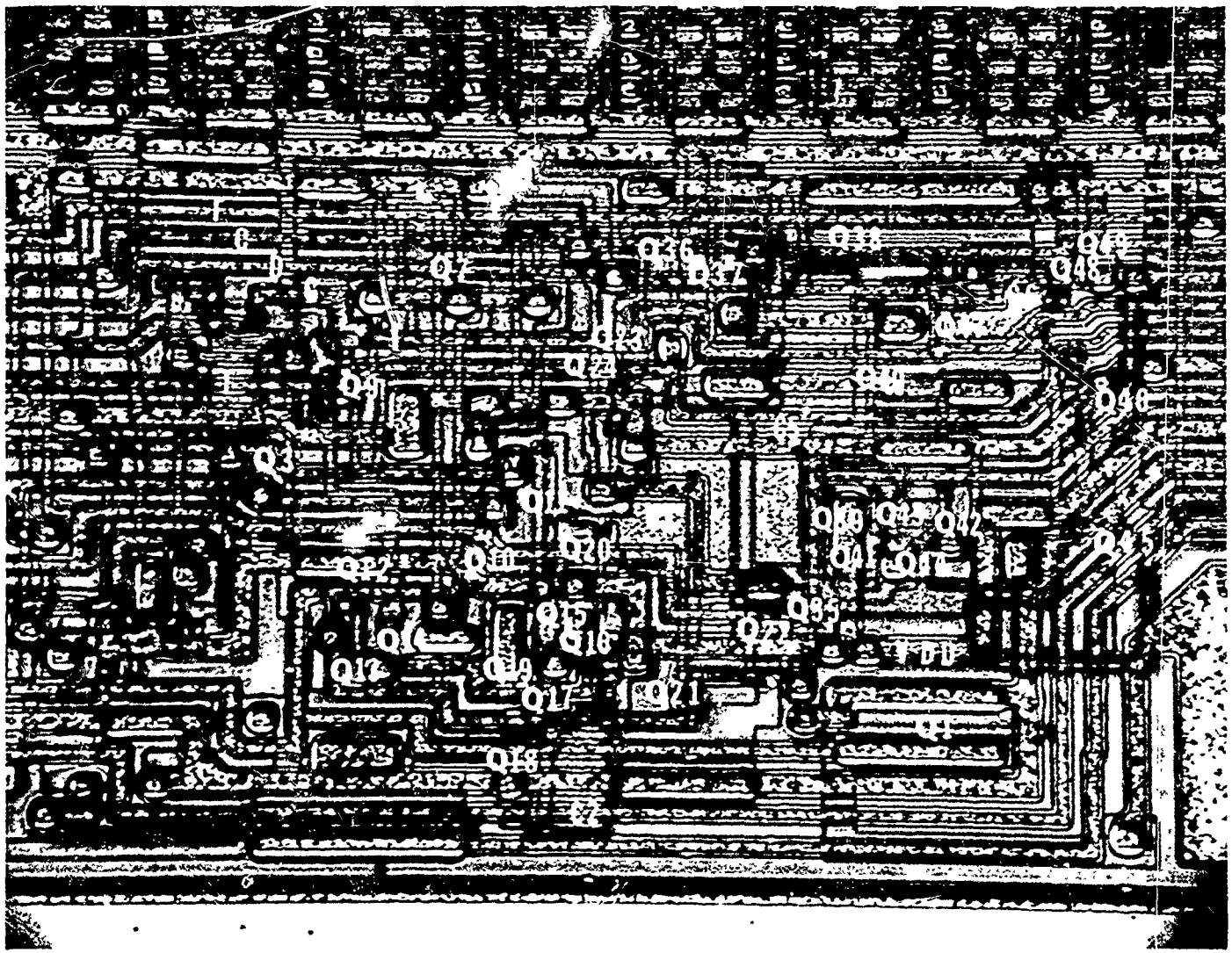

Photo 6-7 Two of Four Light Photographs of the RAS Circuit. Mag. - 300X

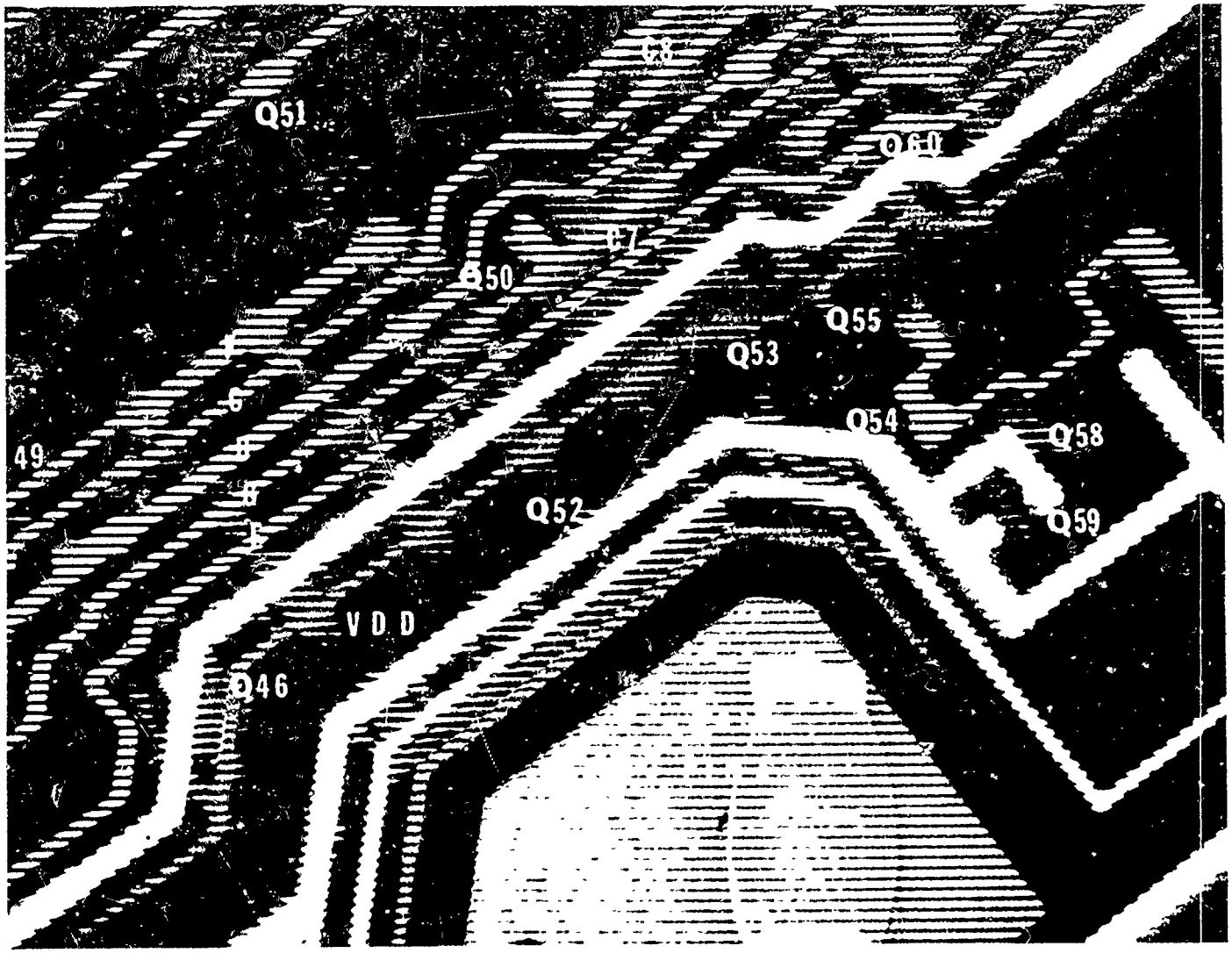

Photo 6-8 Three of Five Voltage Contrast Micrographs of RAS Circuit. 1.3 KV, Mag. - 500X

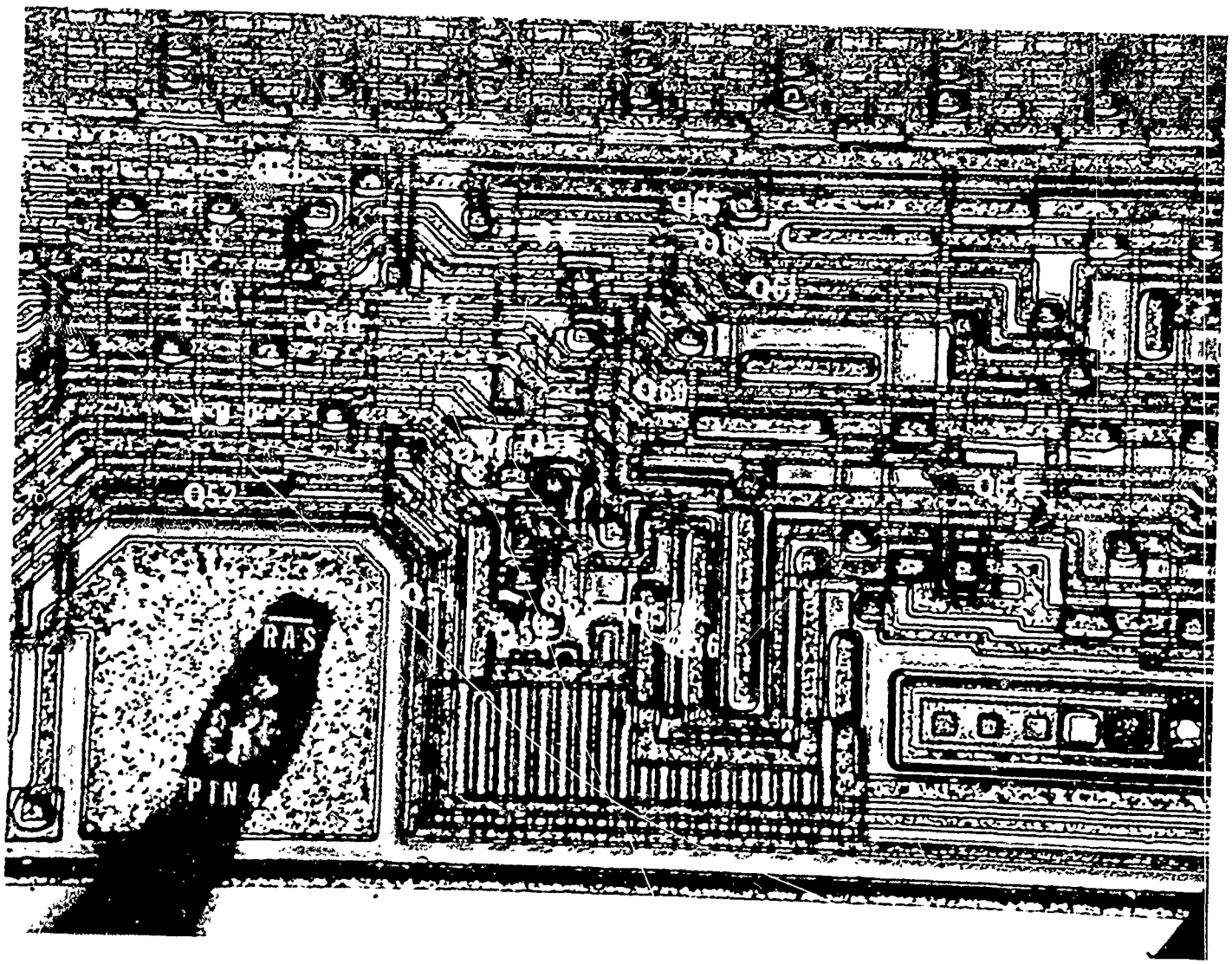

Photo 6-9 Three of Four Light Photographs of the RAS Circuit. Mag. - 300X

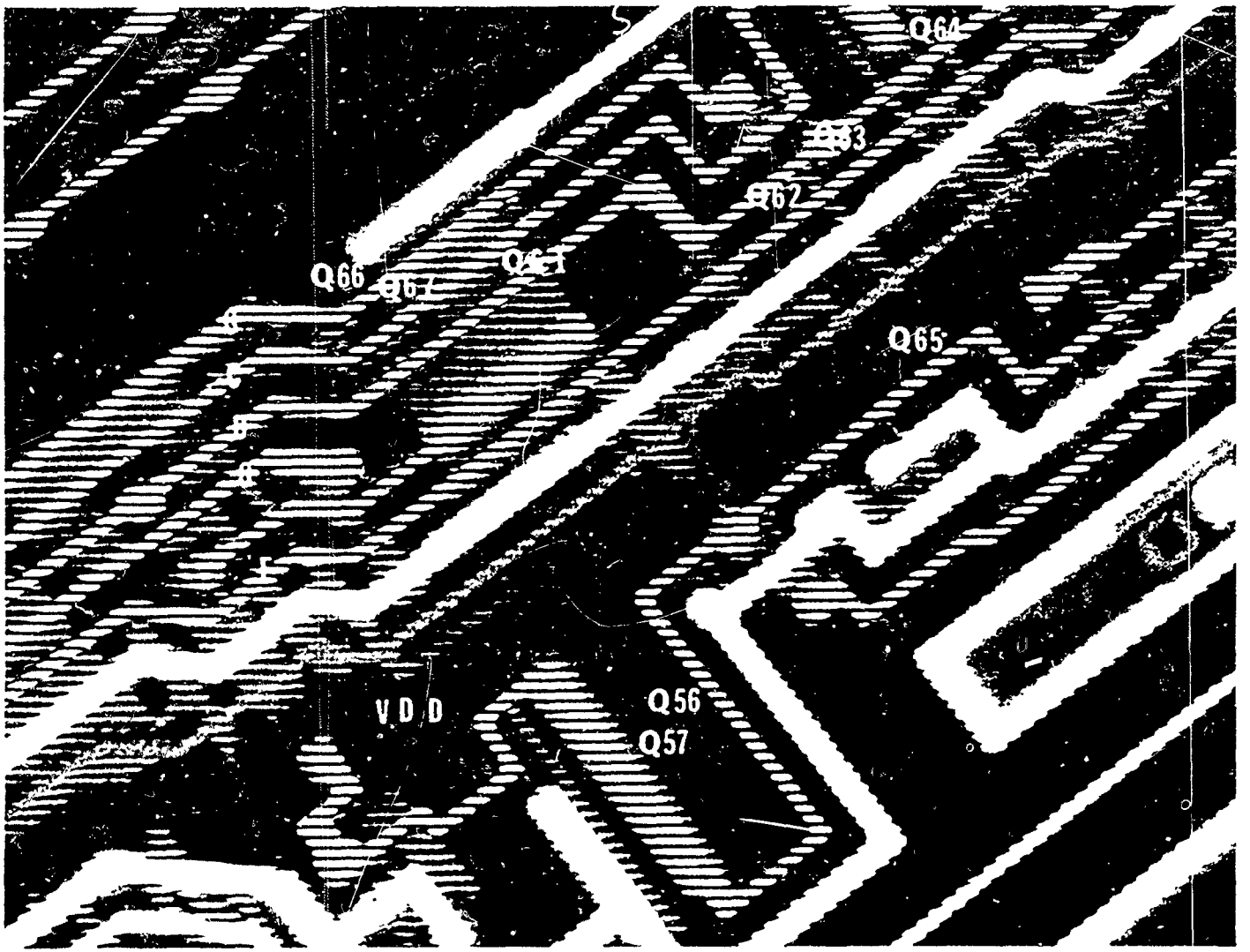

Photo 6-10 Four of Five Voltage Contrast Micrographs of RAS Circuits. 1.3 KV, Mag - 500X

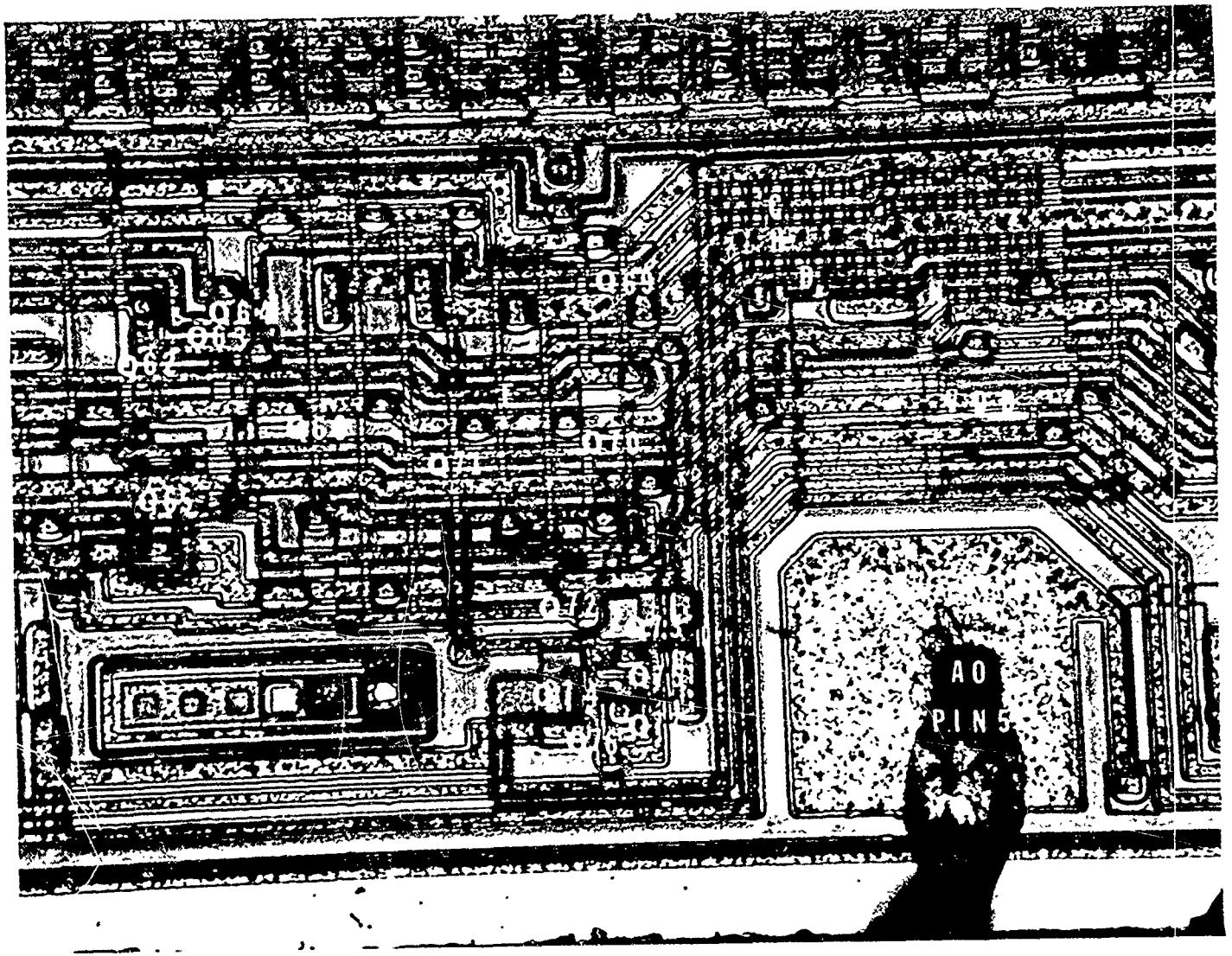

Photo 6-11 Four of Four Light Photographs of RAS Circuit. Mag. - 300X

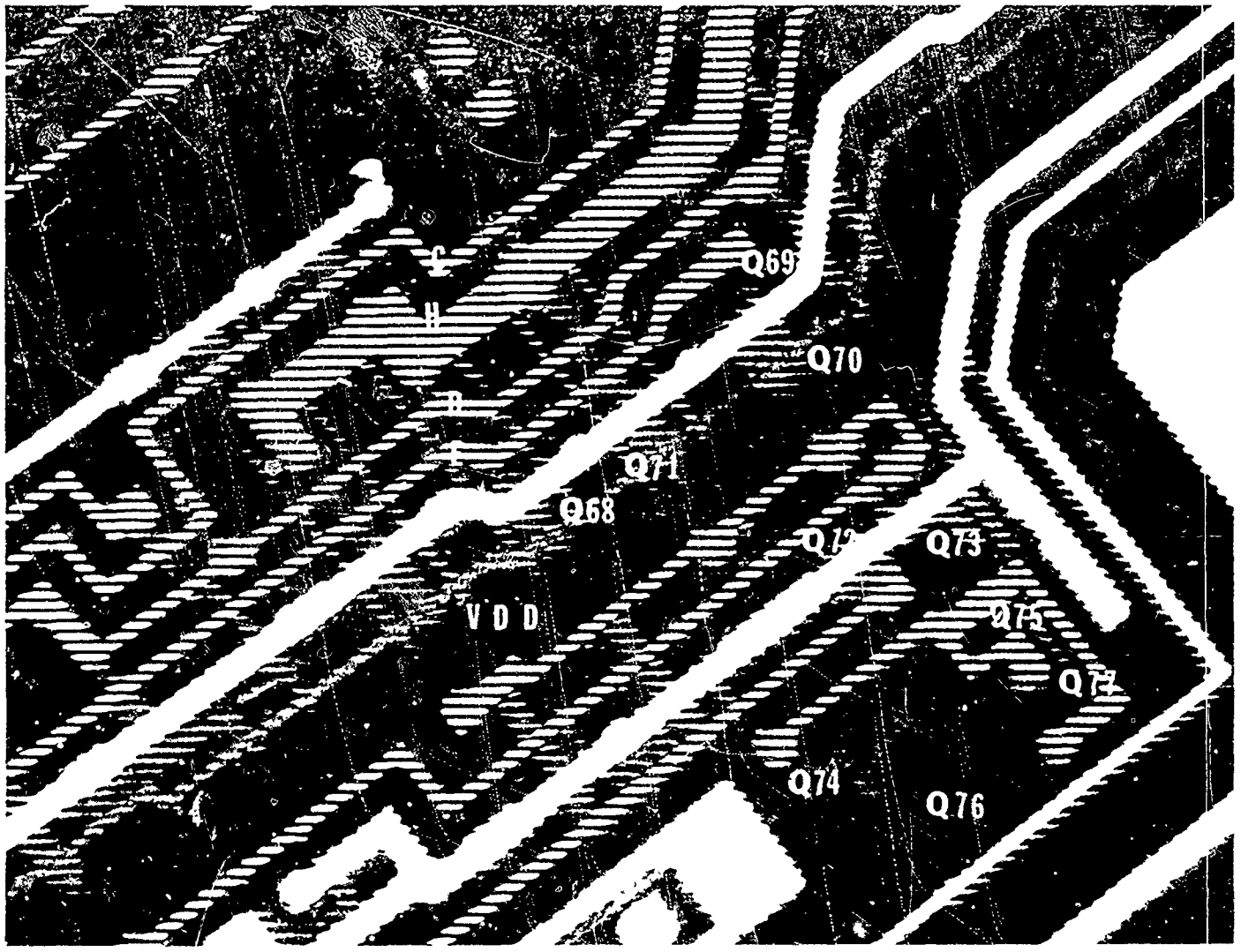

Photo 6-12 Five of Five Voltage Contrast Micrographs of RAS Circuit. 1.3 KV, Mag. - 500X

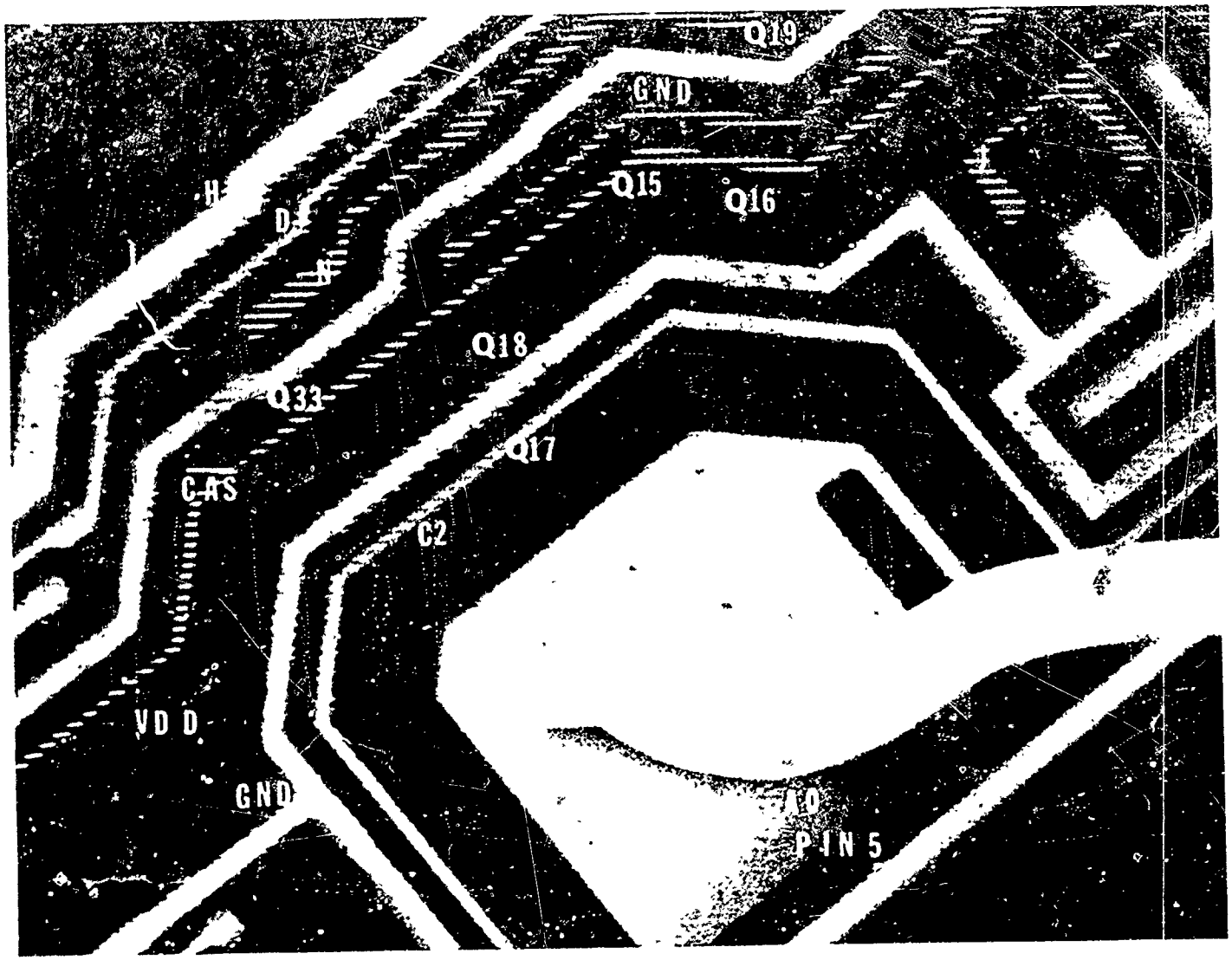

Photo 6-13 One of Four Voltage Contrast Micrographs of CAS Circuit. 1.3 KV, Mag. - 500X

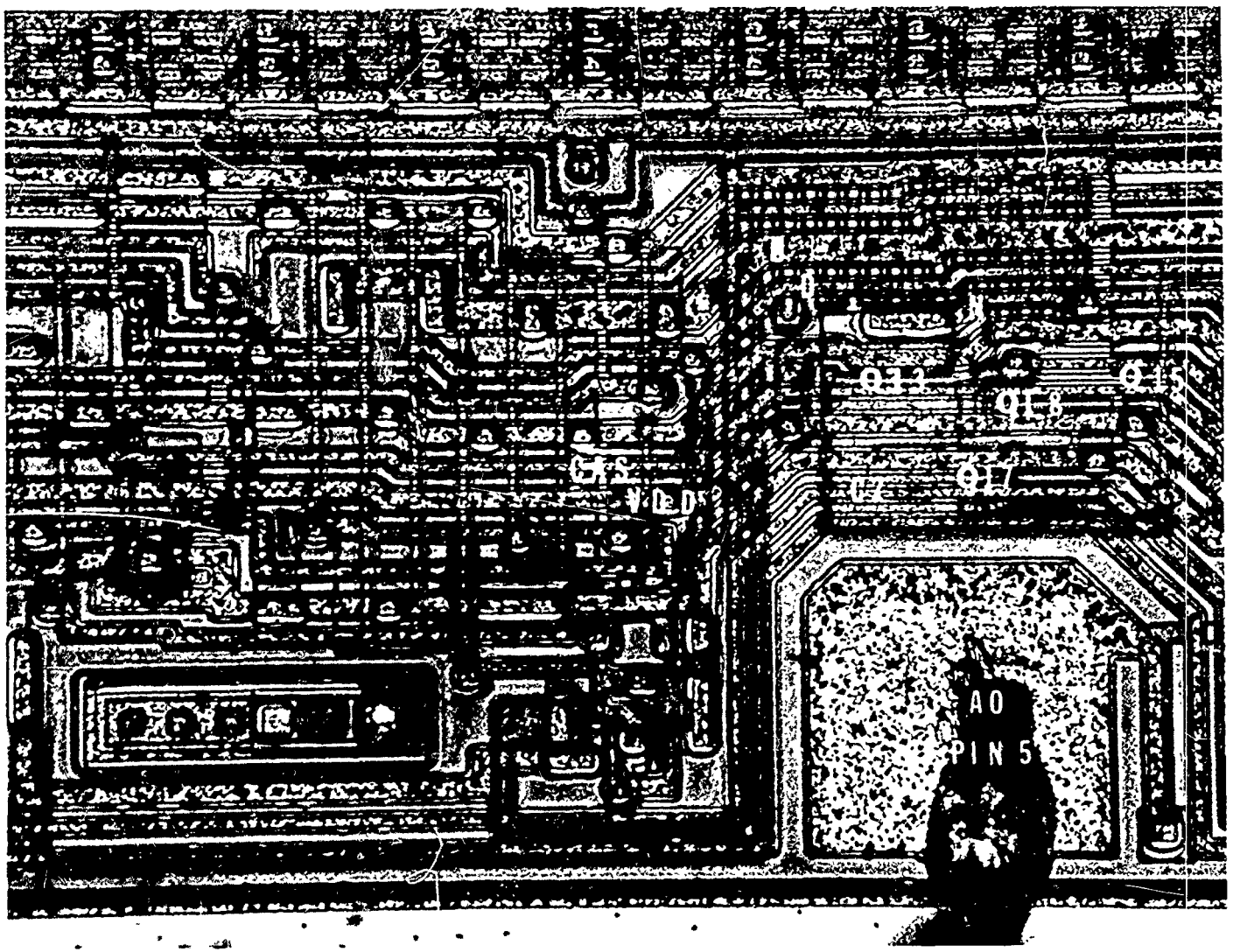

Photo 6-14 One of Three Light Photographs of CAS Circuit. Mag. - 300X

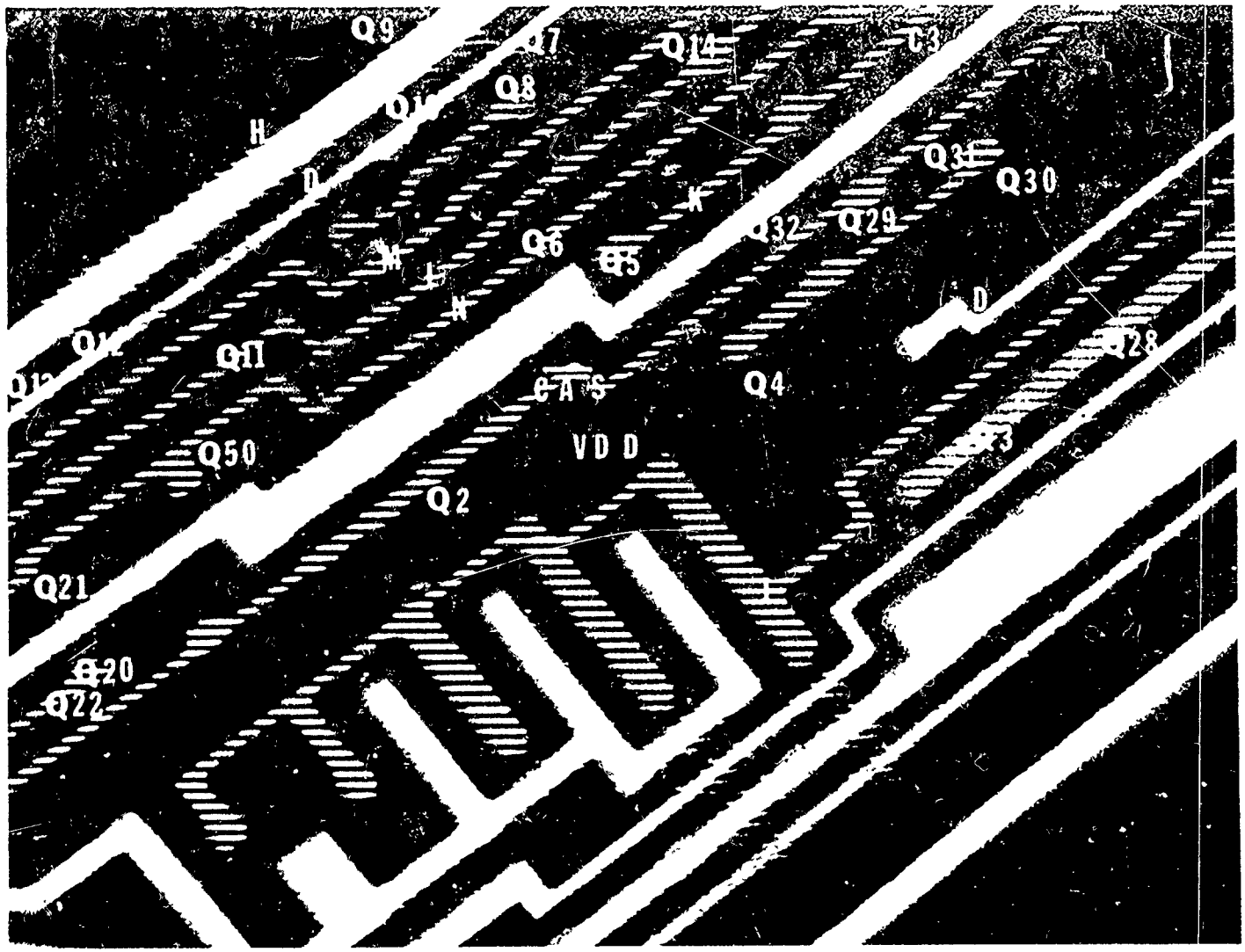

Photo 6-15 Two of Four Voltage Contrast Micrographs of CAS Circuit. 1.3 KV, Mag. - 500X

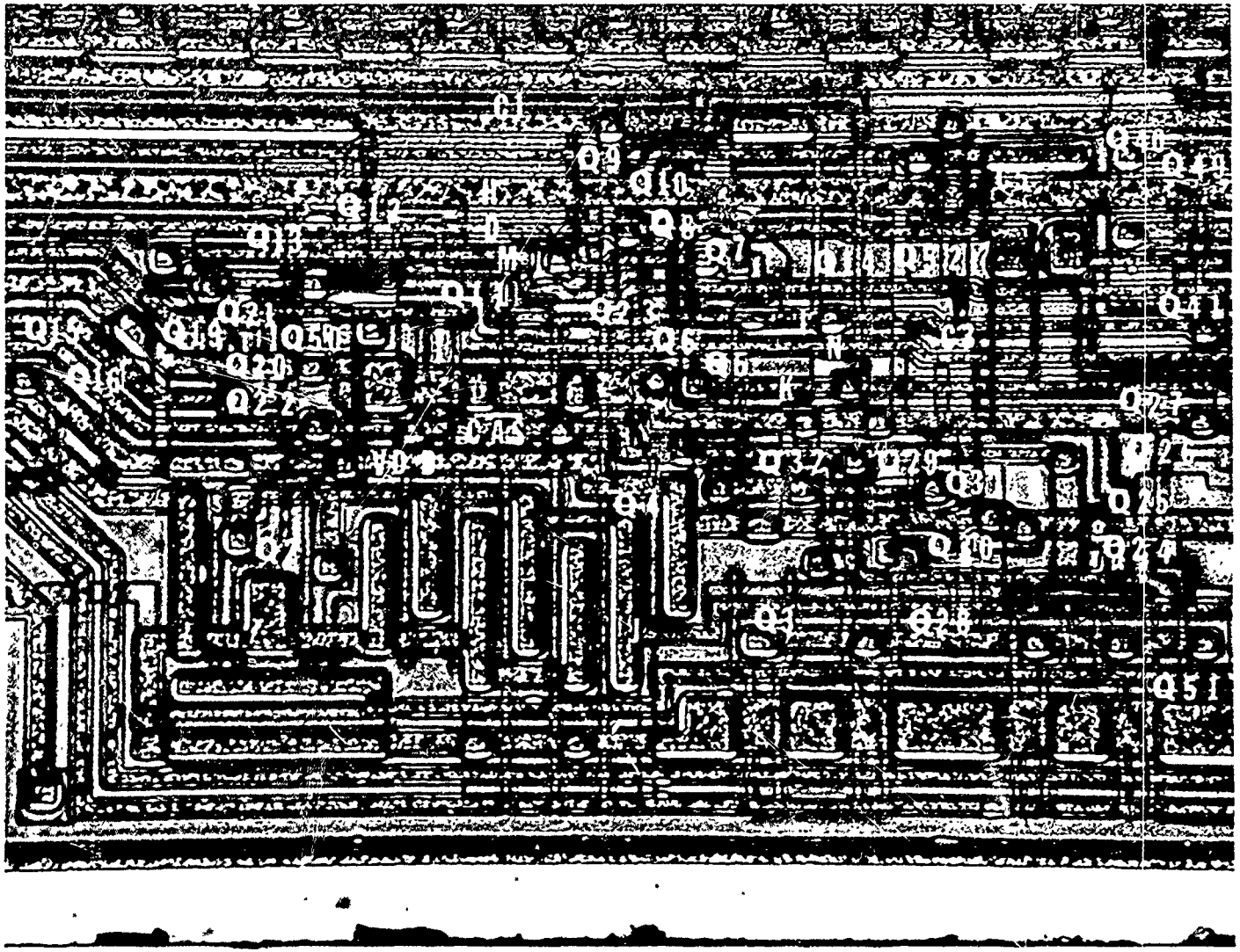

Photo 6-16 Two of Three Light Photographs of CAS Circuit. Mag. - 300X

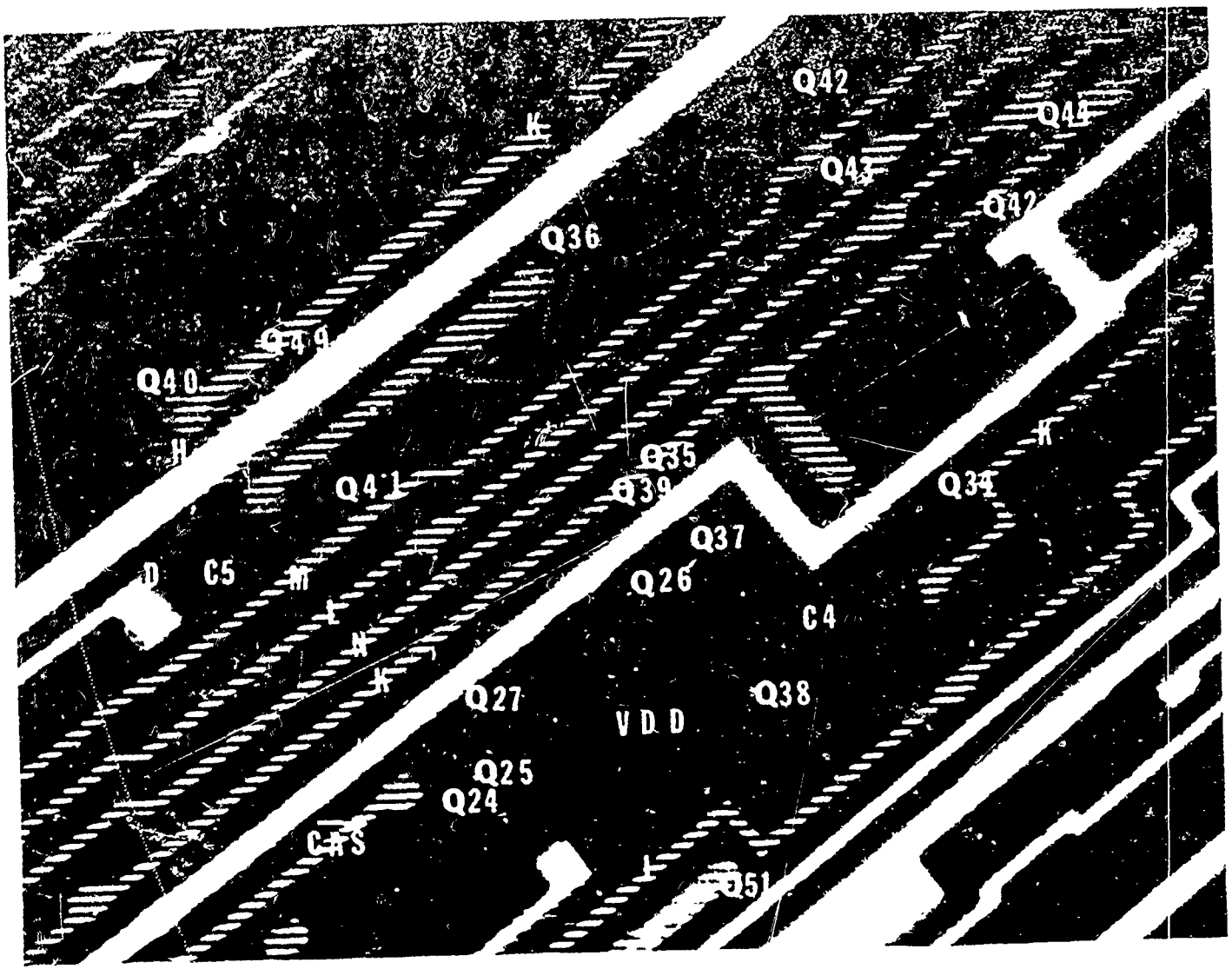

Photo 6-17 Three of Four Voltage Contrast Micrographs of CAS Circuit. 1.3 KV, Mag. - 500X

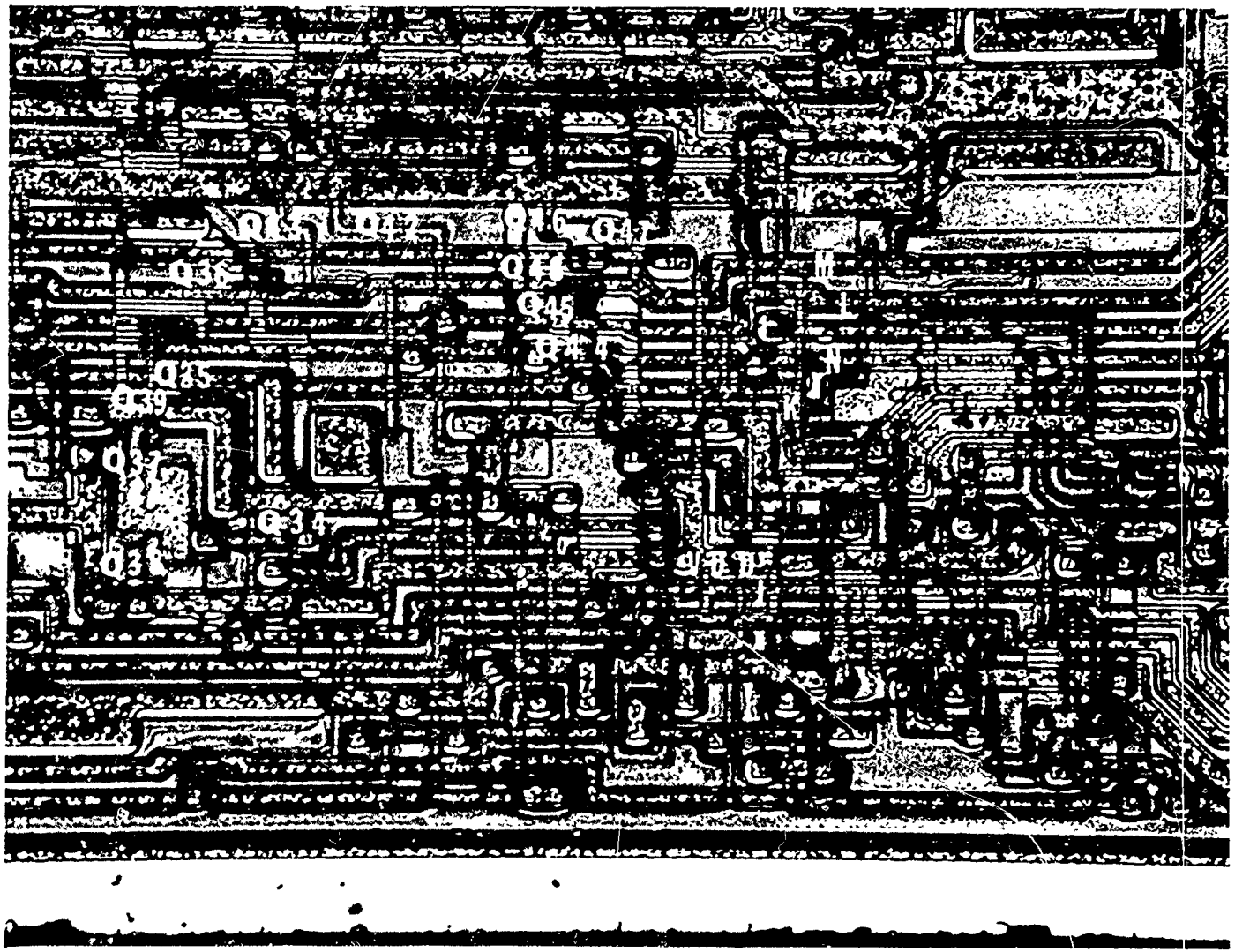

Photo 6-18 Three of Three Light Photographs of CAS Circuit. Mag. - 300X

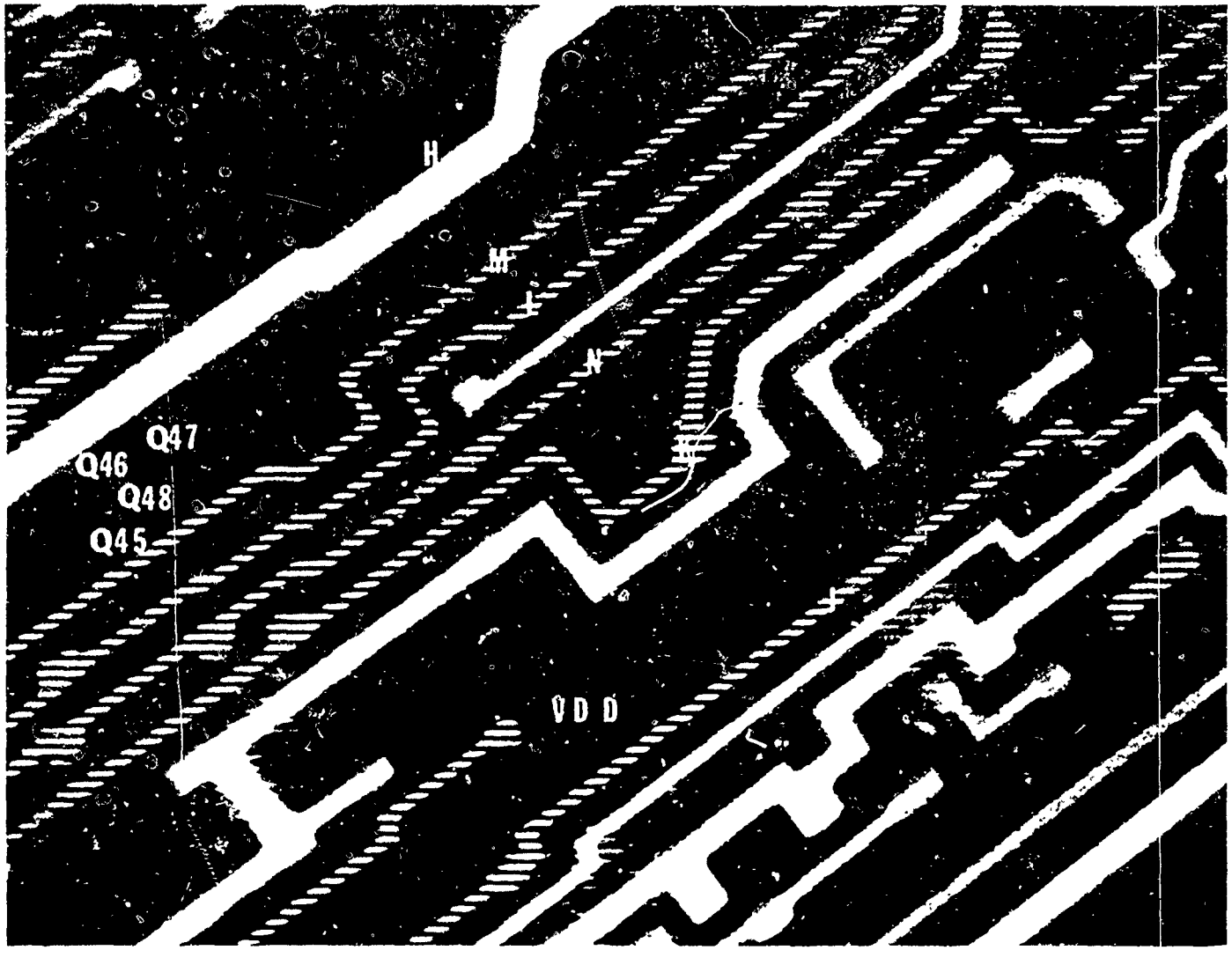

Photo 6-19 Four of Four Voltage Contrast Micrographs of CAS Circuit. 1.3 KV, Mag. - 500X

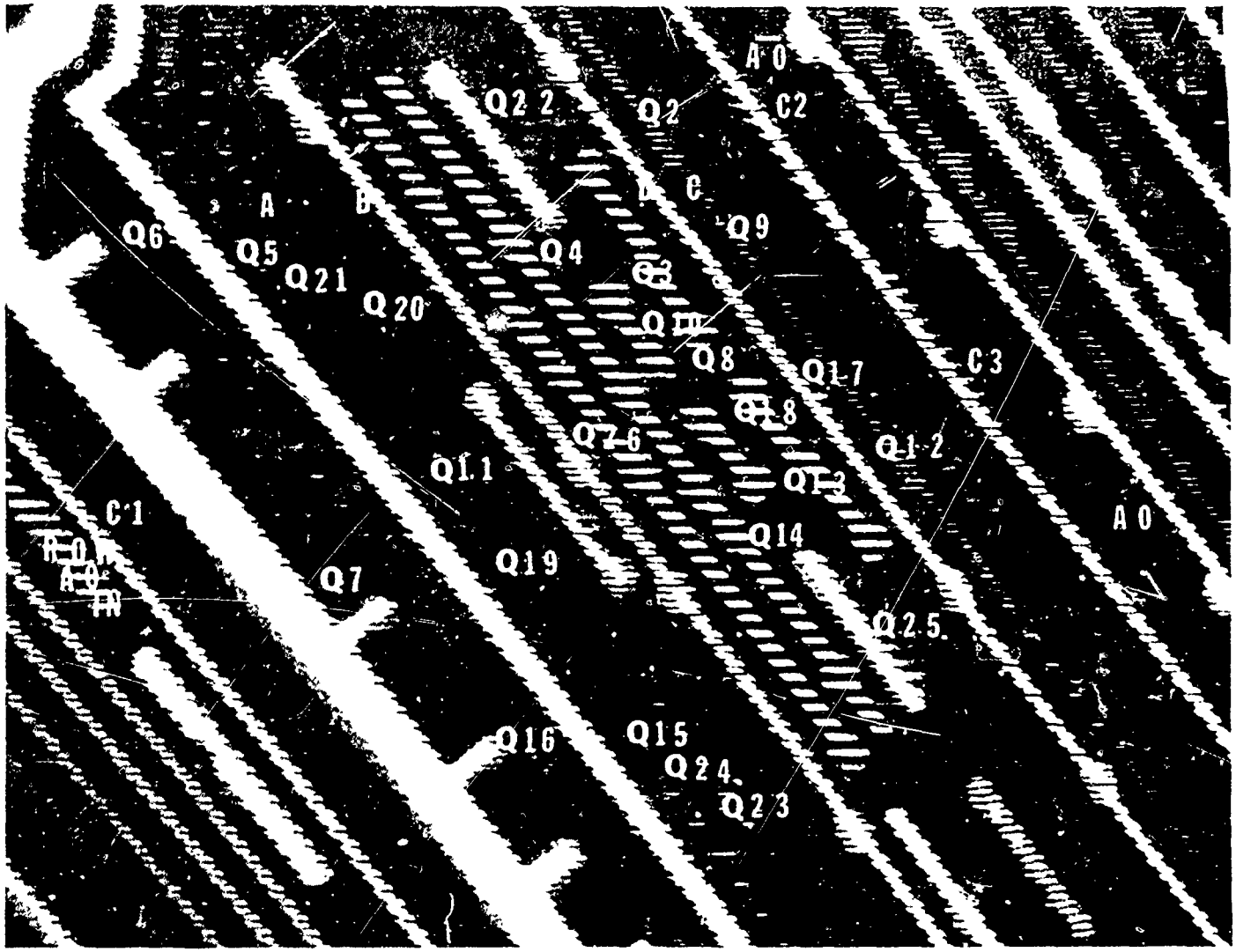

Photo 6-20 Voltage Contrast Micrograph of the AO Row Address Buffer/Latch Circuit. 1.3 KV, Mag. - 500X

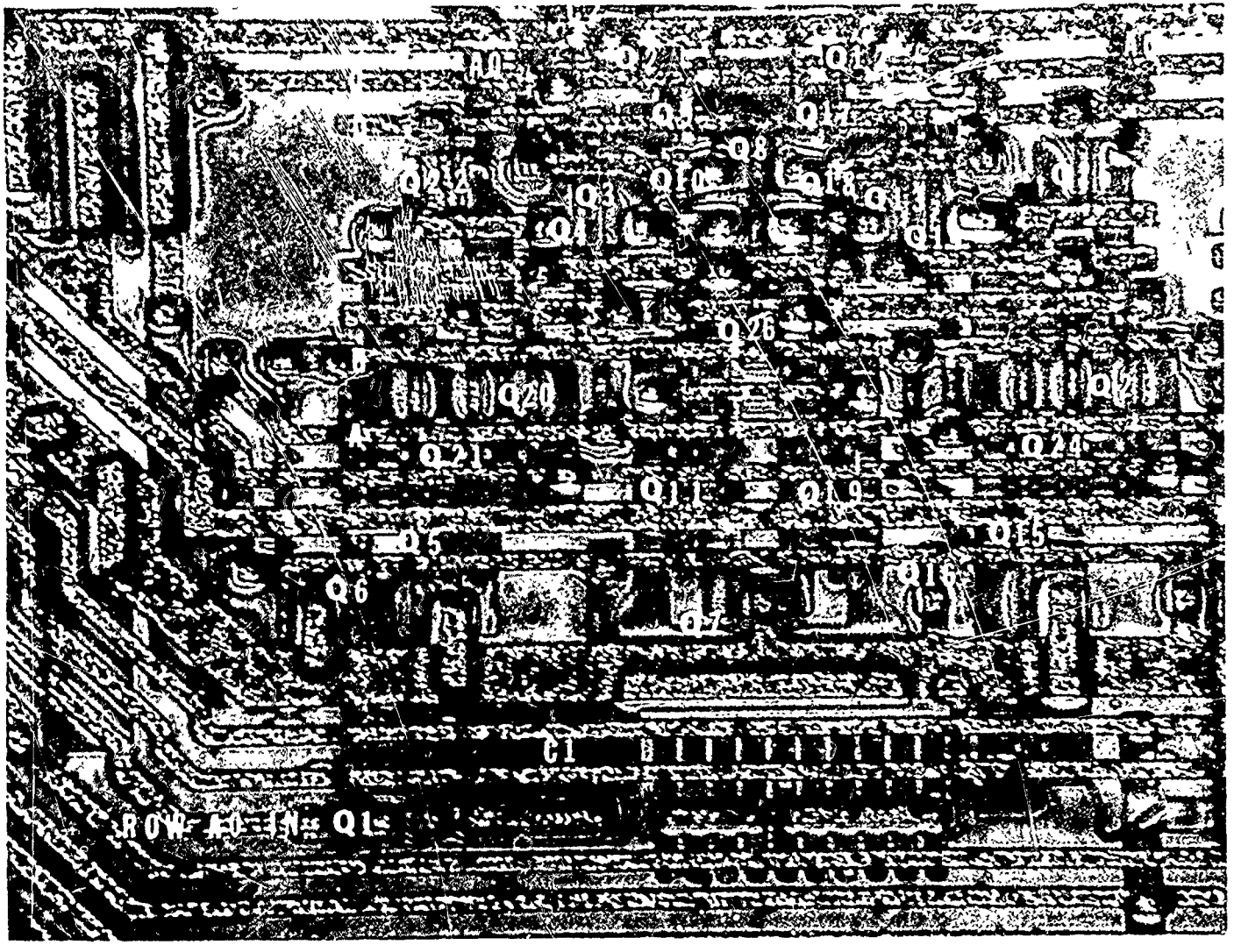

Photo 6-21 Light Photograph of the A0 Row Address Buffer/Latch Circuit. Mag. - 450X

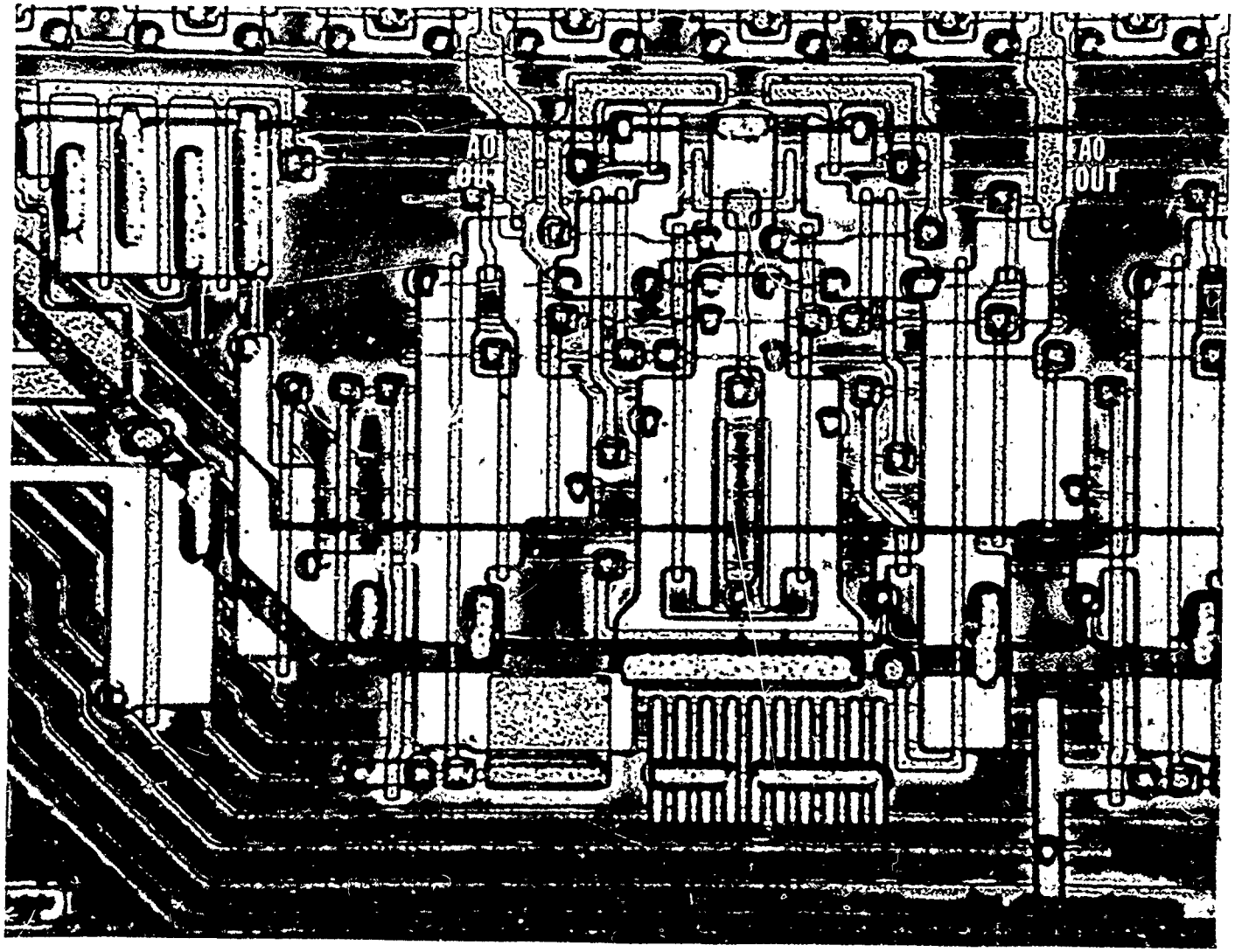

Photo 6-22 Light Photograph of the A0 Row Address Buffer/Latch Circuit with the Metallization Removed. Mag. - 450X

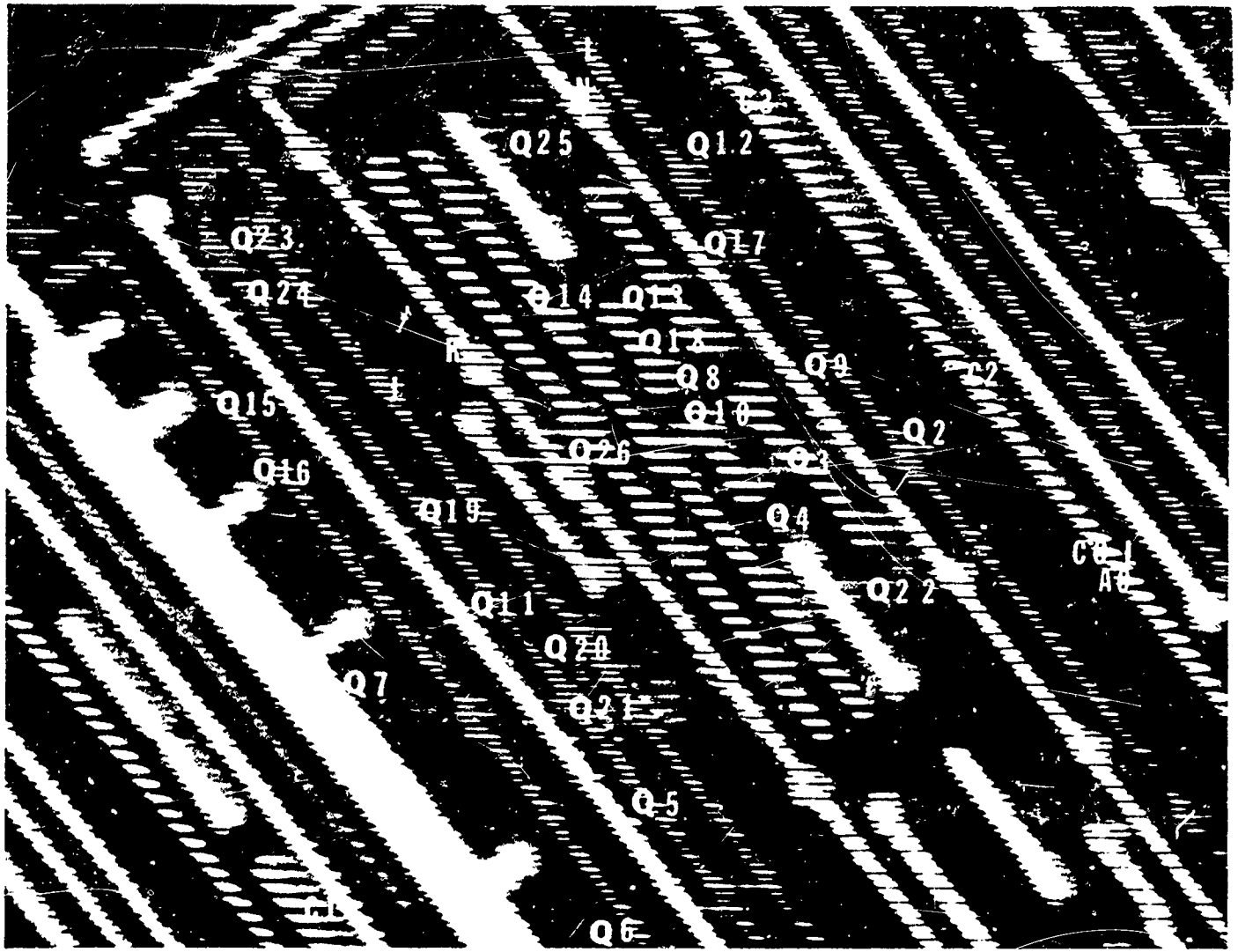

Photo 6-23 Voltage Contrast Micrograph of the AO Column Address Buffer/Latch Circuit. 1.3 KV, Mag. - 500X

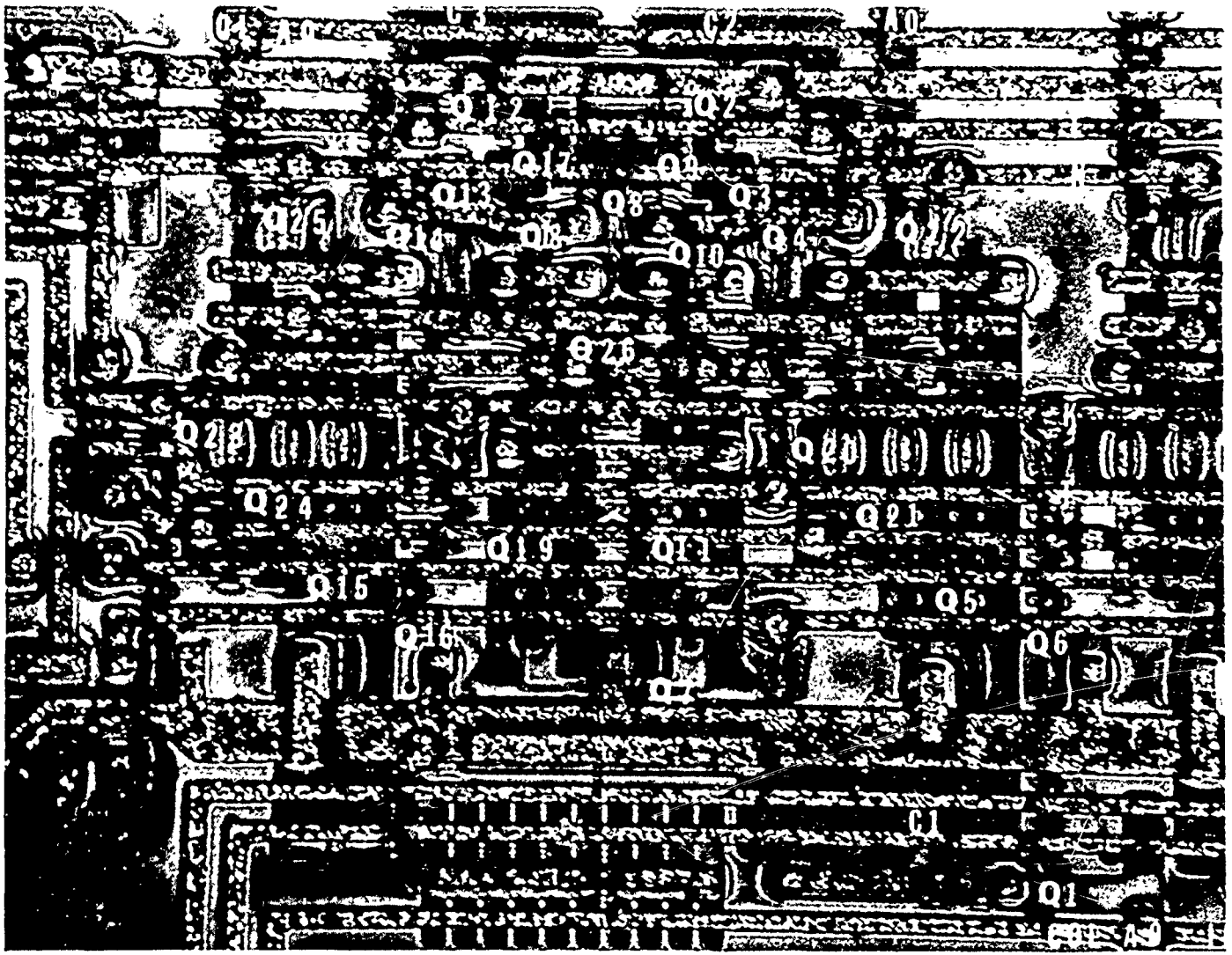

Photo 6-24 Light Photograph of AO Column Address Buffer/Latch Circuit. Mag. - 450X

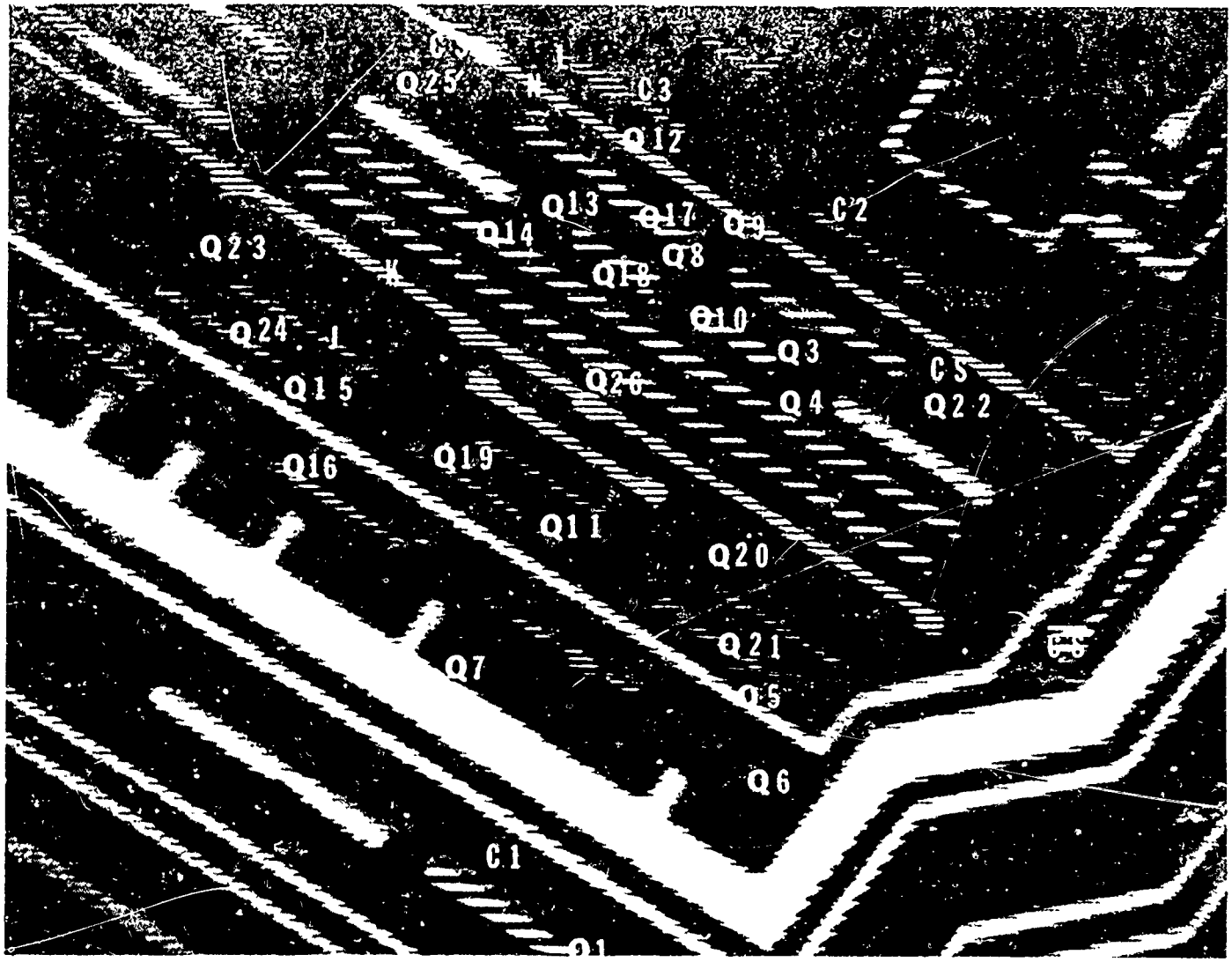

Photo 6-25 Voltage Contrast Micrograph of the Chip Select Buffer/Latch Circuit. 1.3 KV, Mag. - 500X

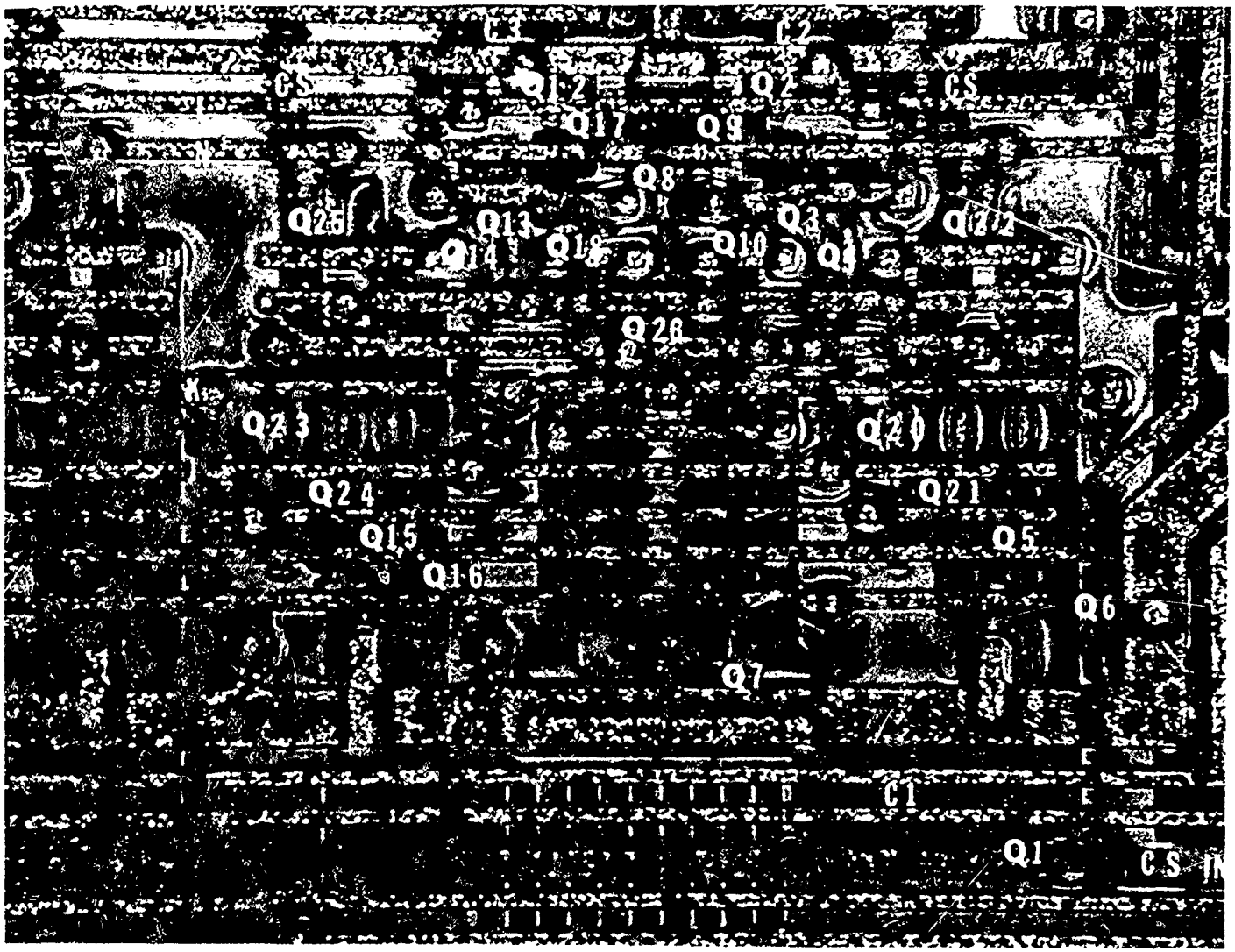

Photo 6-26 Light Photograph of the Chips Select Buffer/Latch Circuit. Mag. - 450X

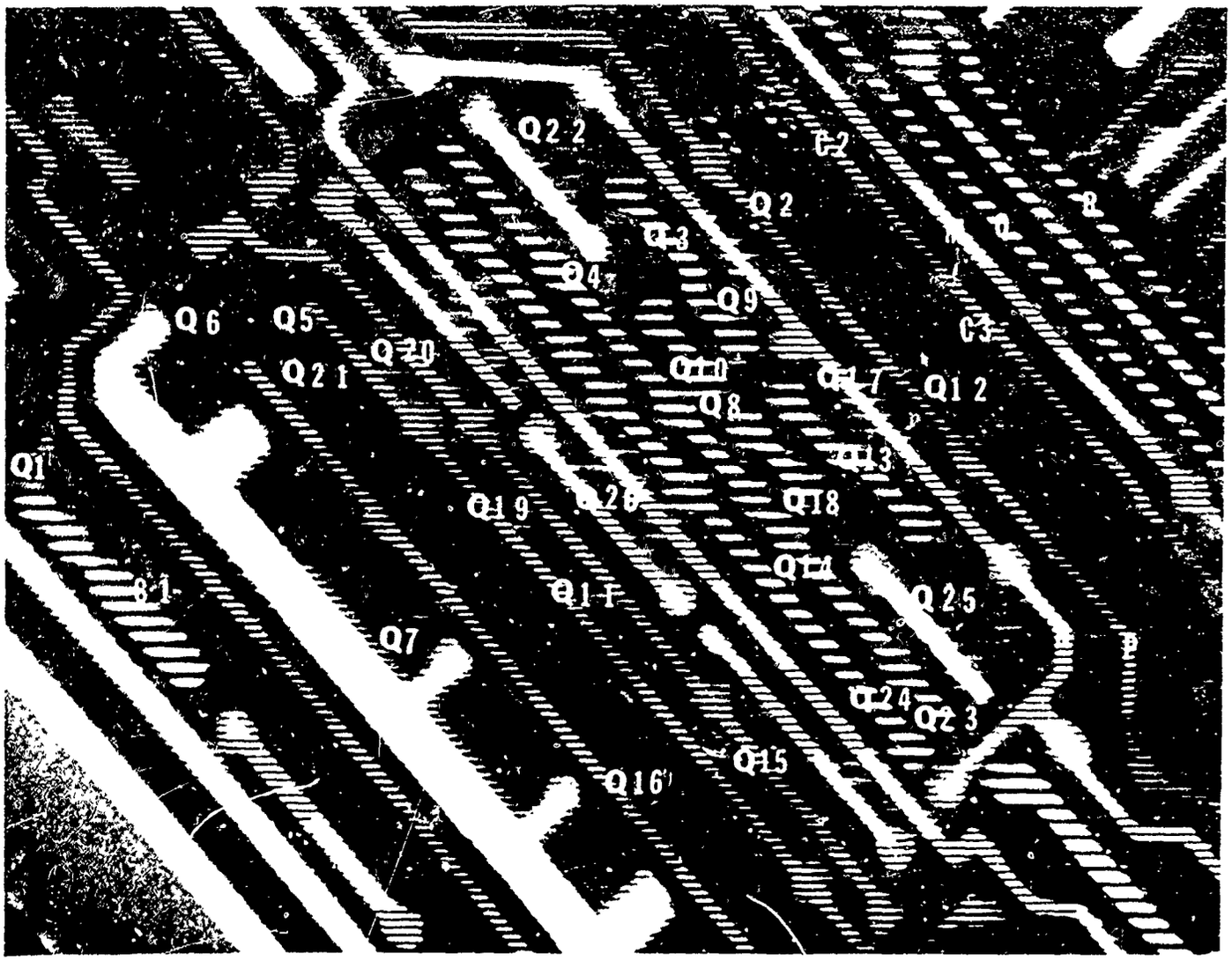

Photo 6-27 Voltage Contrast Micrograph of the Data in Buffer/Latch Circuit. 1.3 KV, Mag. - 500X

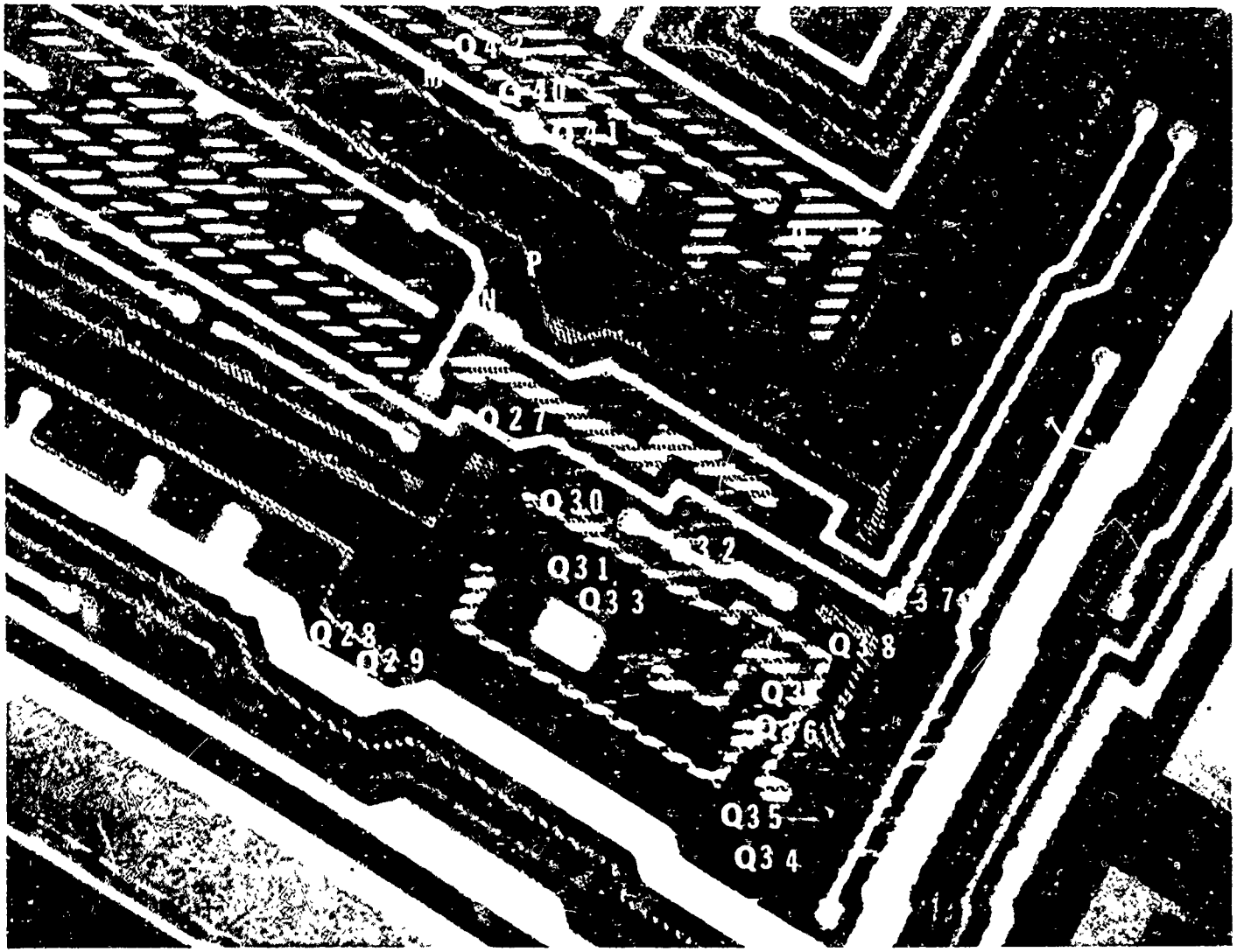

Photo 6-28 Voltage Contrast Micrograph of the Data in Latch/Driver Circuit. 1.3 KV, Mag. - 340X

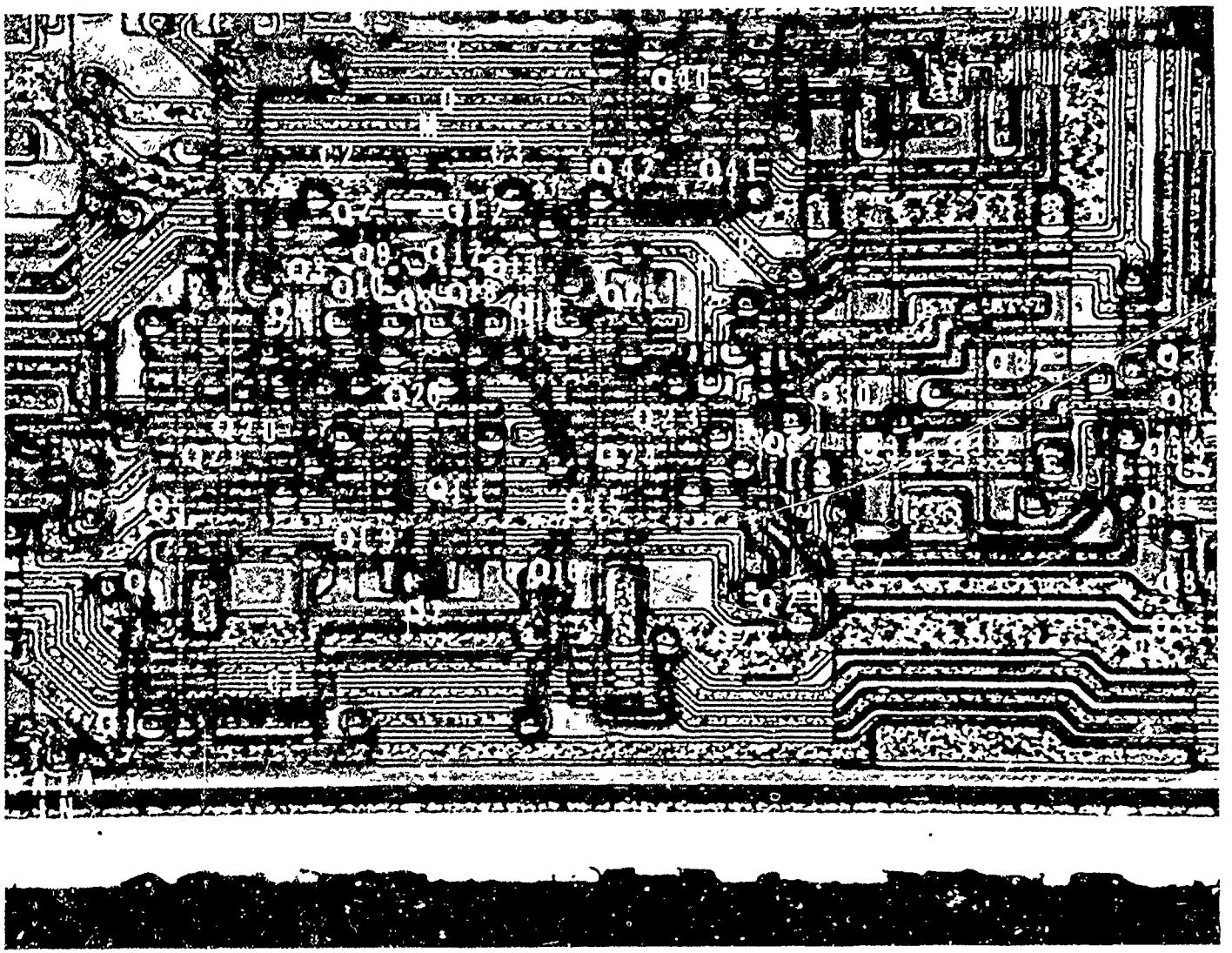

Photo 6-29 Light Photograph of the Data in Buffer/Latch/Driver Circuit. Mag. - 300X

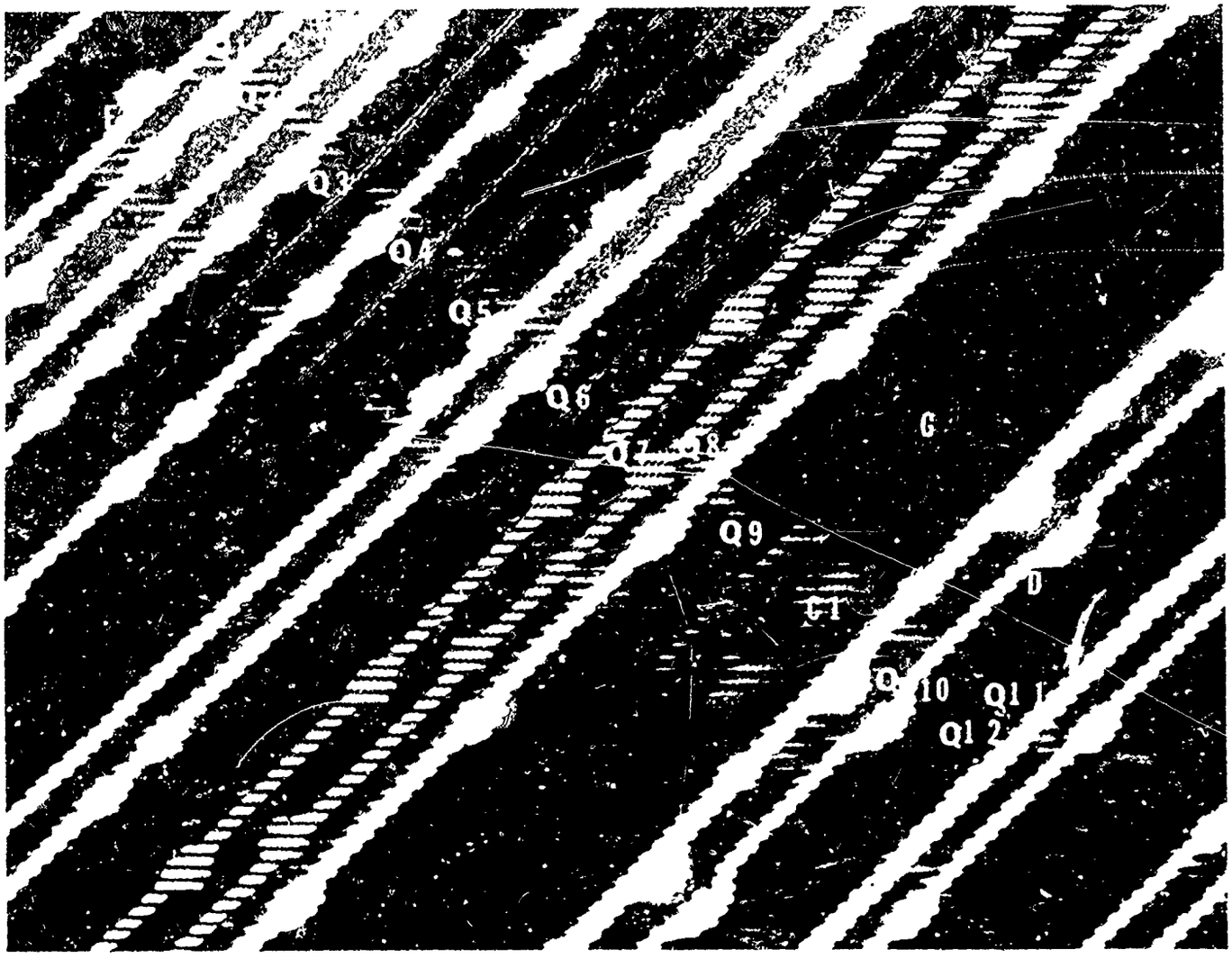

Photo 6-30 Voltage Contrast Micrograph of the Row Decode Circuit. 1.3 KV, Mag. - 575X

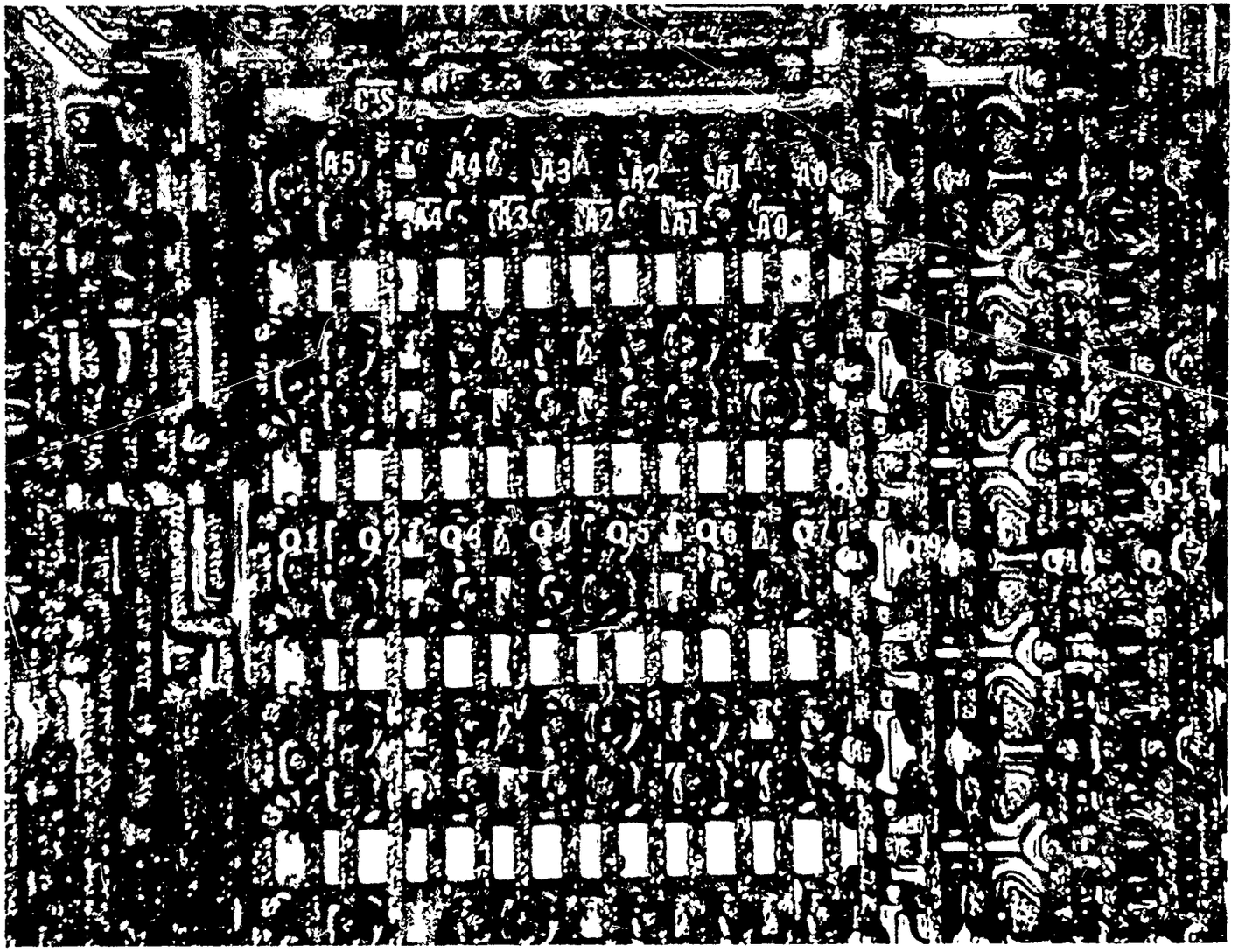

Photo 6-31 Light Photograph of the Row Decode Circuit. Mag. - 36X

Photo 6-32 Voltage Contrast Micrograph of a Typical Memory Cell. 1.3 KV, Mag. - 775X

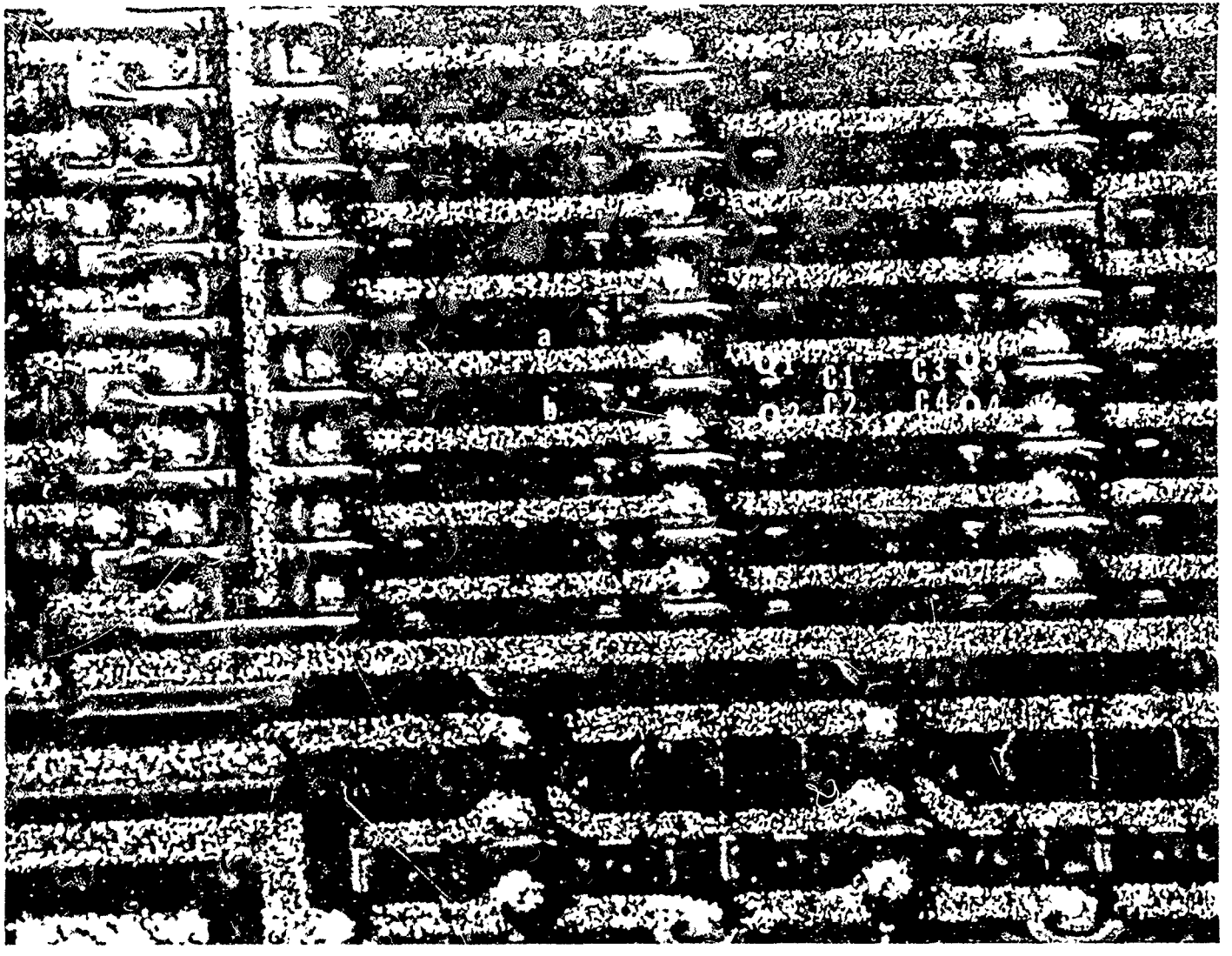

Photo 6-33 Light Photograph of a Typical Memory Cell. Mag. - 775X

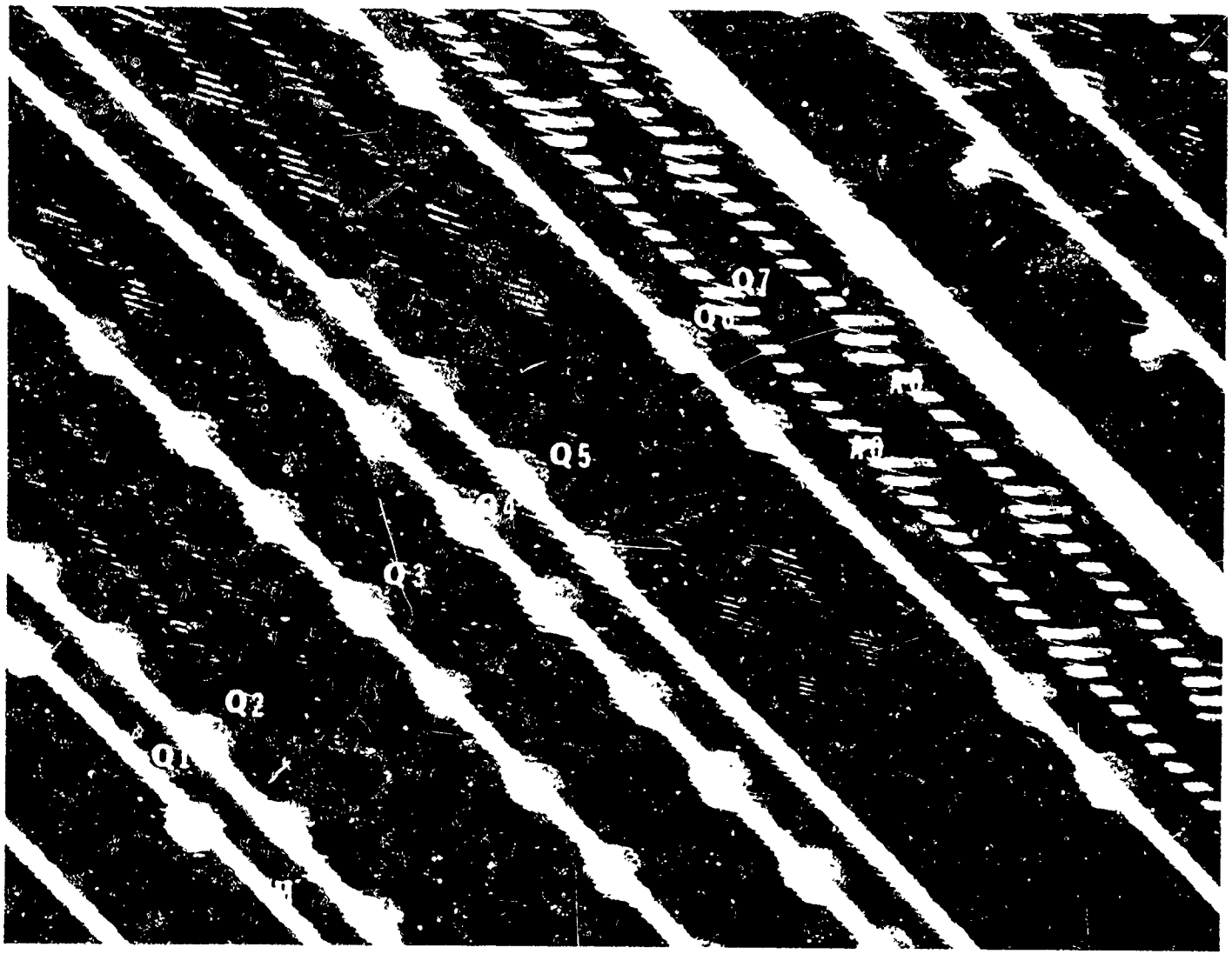

Photo 6-34 Voltage Contrast Micrograph of the Column Decode Circuit. 1.3 KV, Mag. - 700X

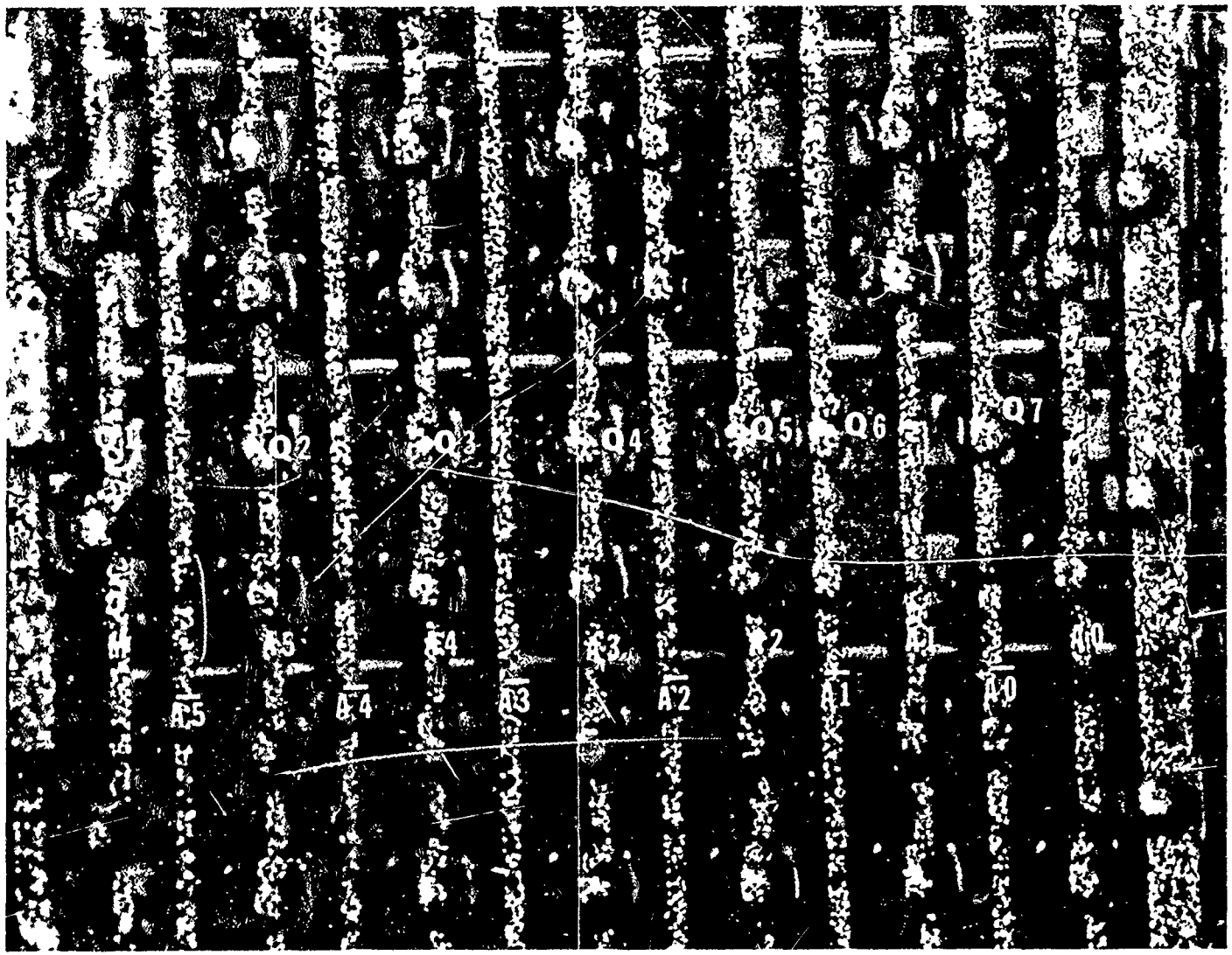

Photo 6-35 Light Photograph of the Column Decode Circuit. Mag. - 775X

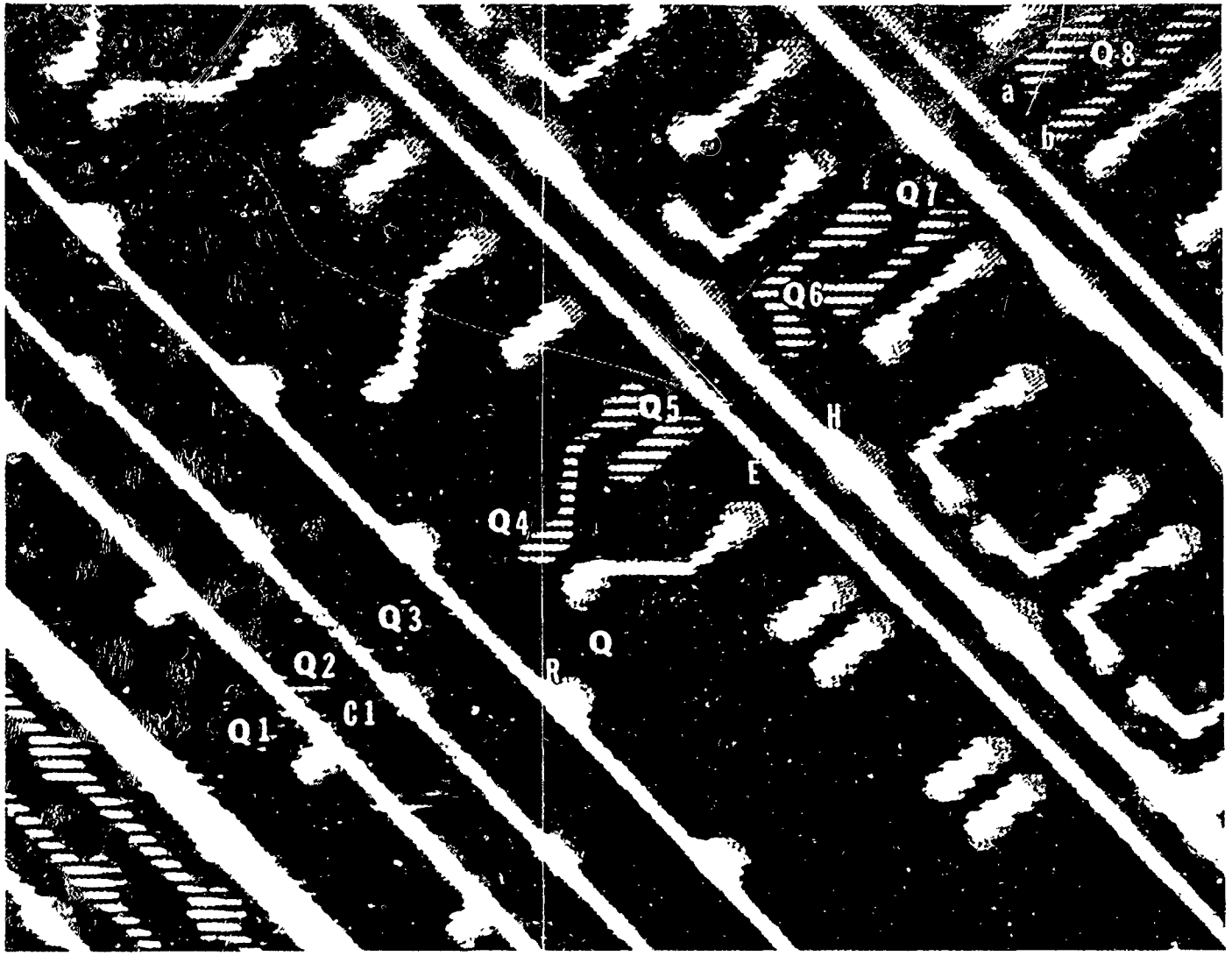

Photo 6-36 Voltage Contrast Micrograph of a Column Sense Amplifier. 1.3 KV, Mag. - 620X

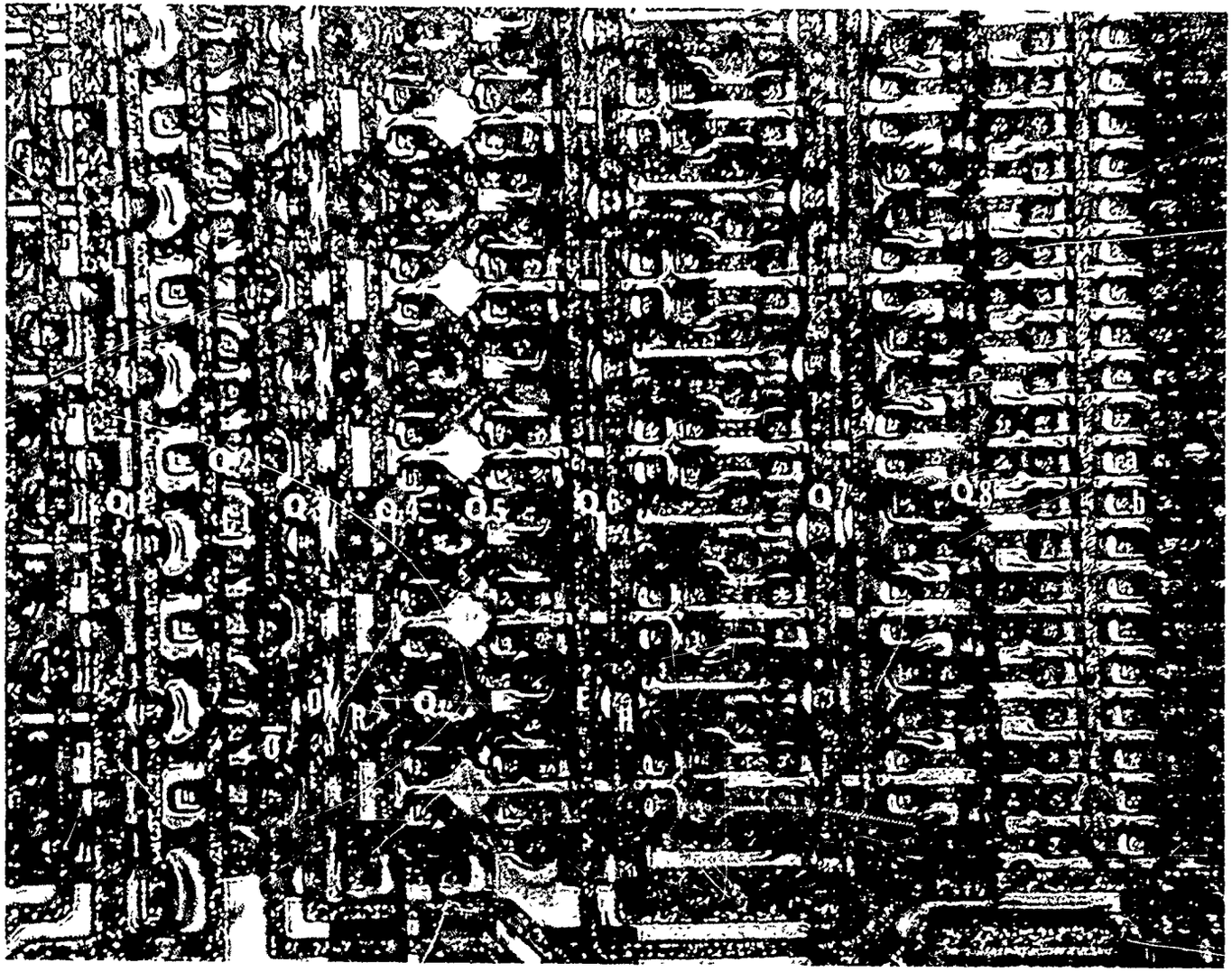

Photo 6-37 Light Photograph of a Column Sense Amplifier. Mag. - 360X

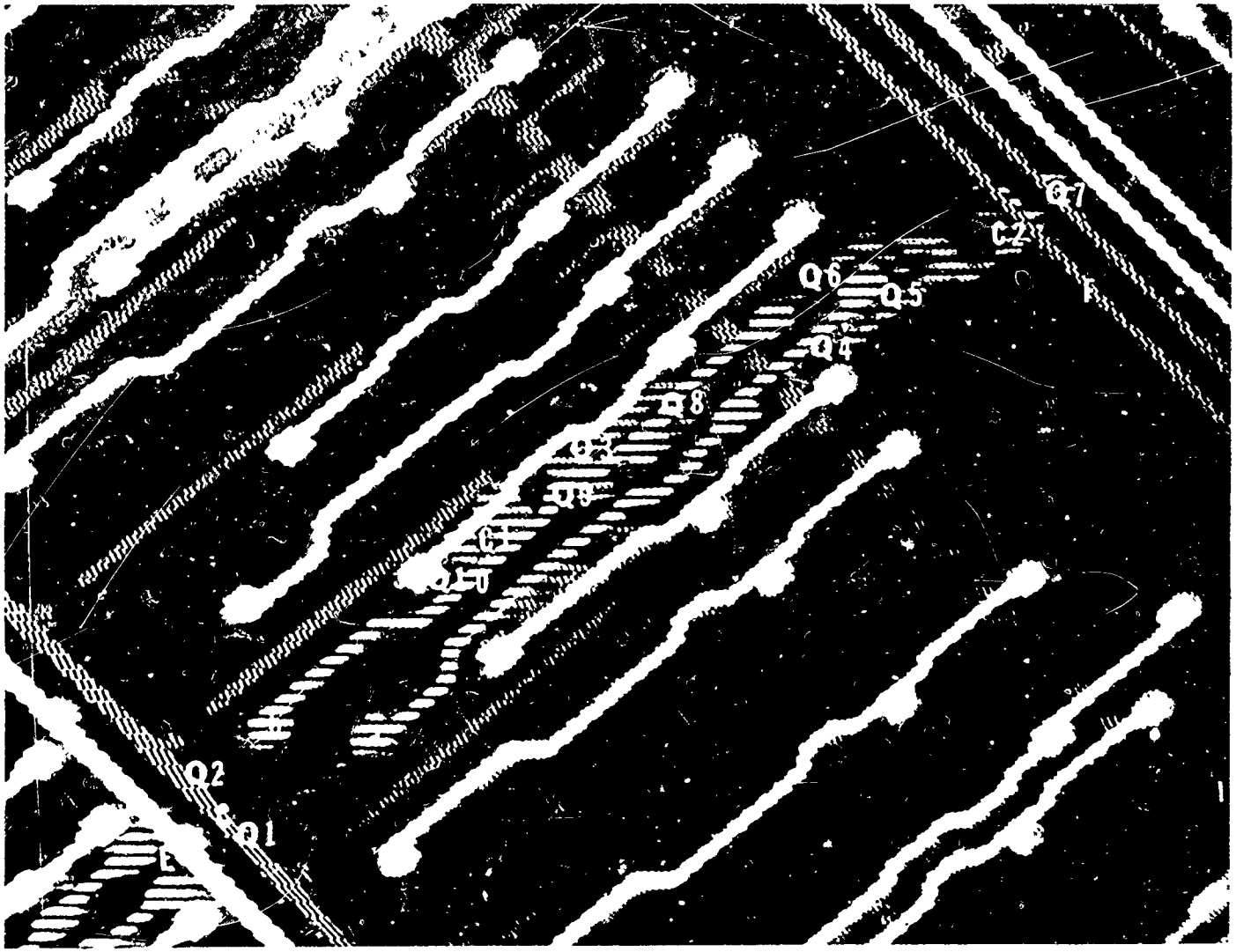

Photo 6-38 Voltage Contrast Micrograph of a Column Precharge/Refresh Circuit. 1.3 KV, Mag. - 500X

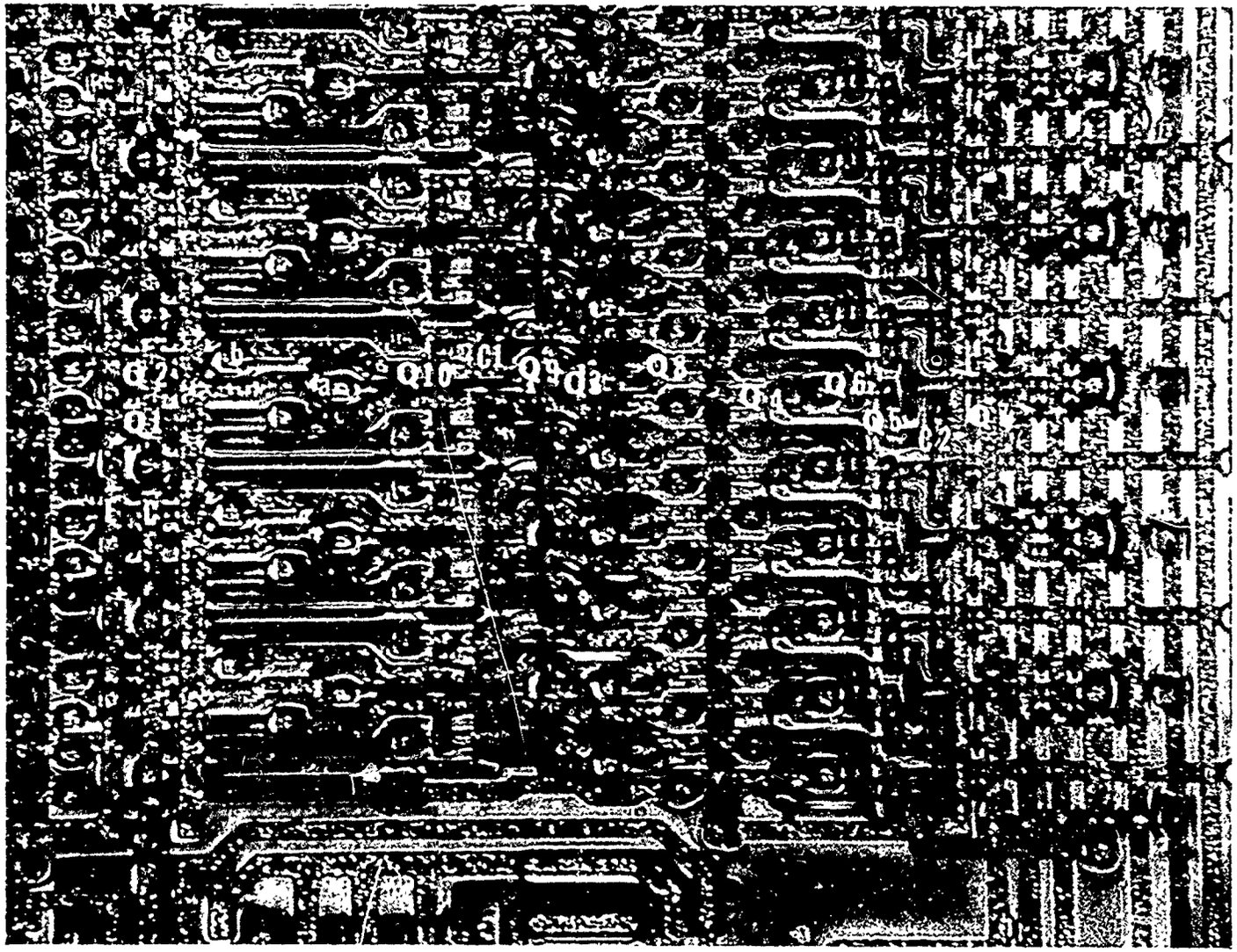

Photo 6-39 Light Photograph of a Column Precharge/Refresh Circuit. Mag. - 360X

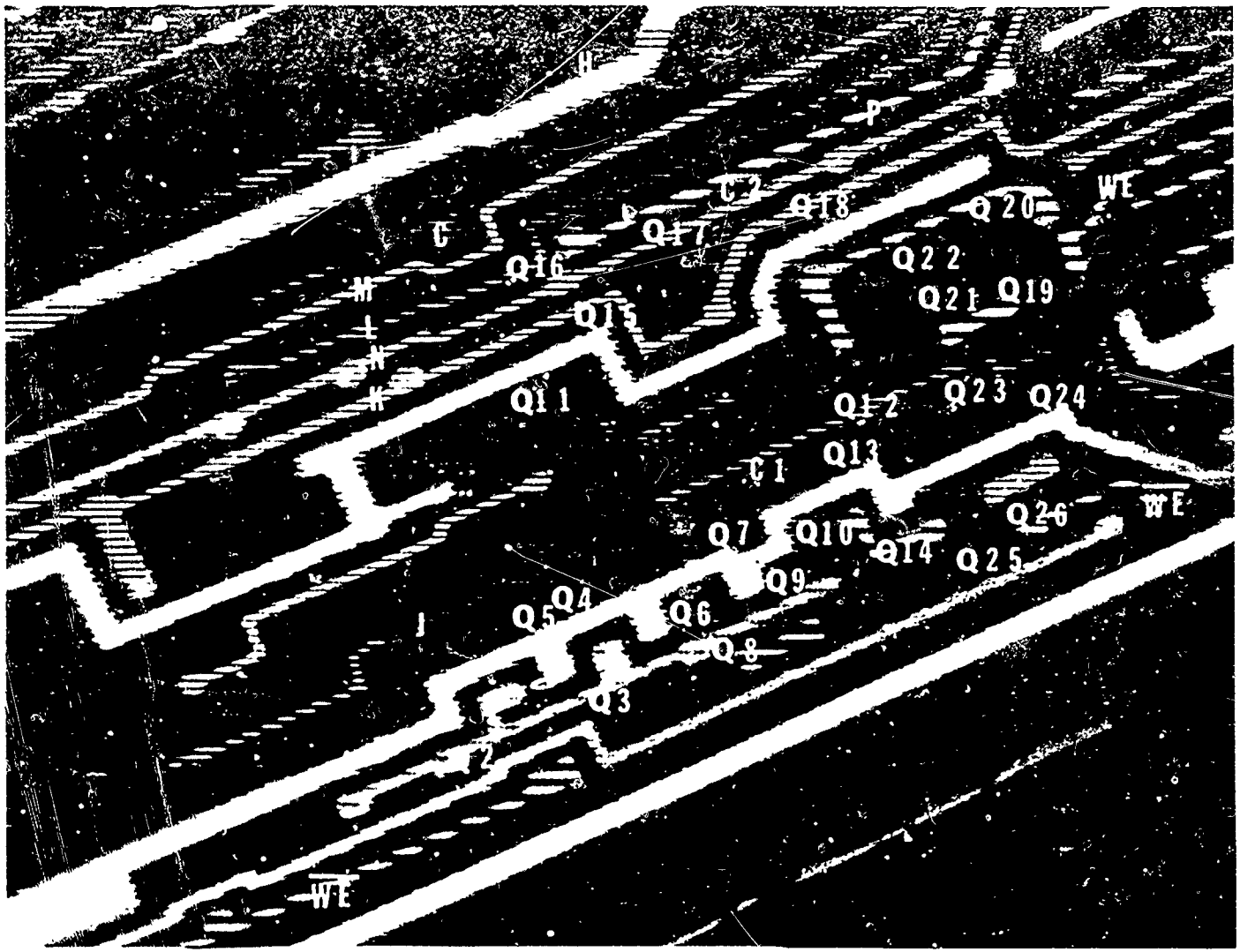

Photo 6-40 Voltage Contrast Micrograph of the Write Enable Buffer. 1.3 KV, Mag. - 370X

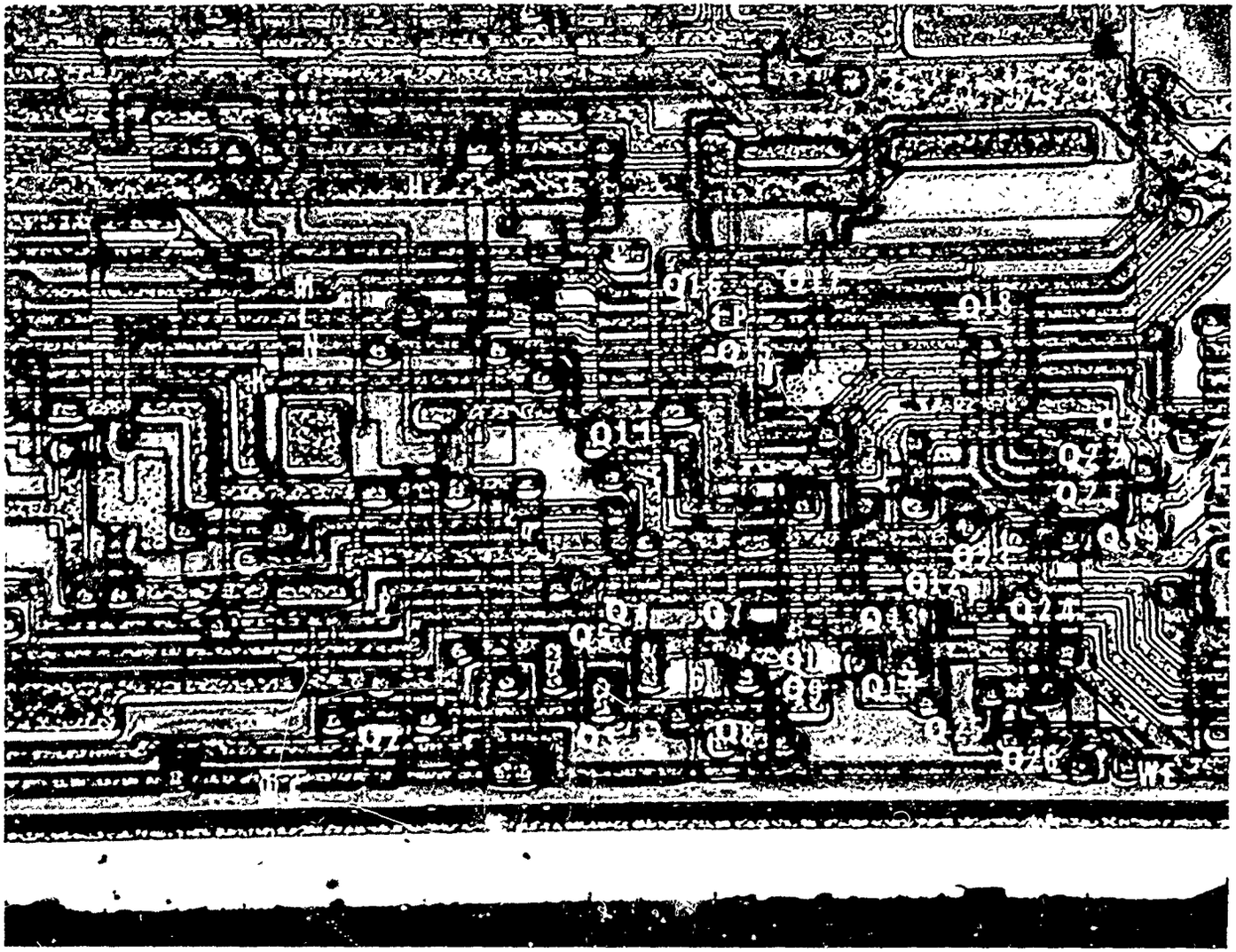

Photo 6-41 Light Photograph of the Write Enable Buffer. Mag. - 300X

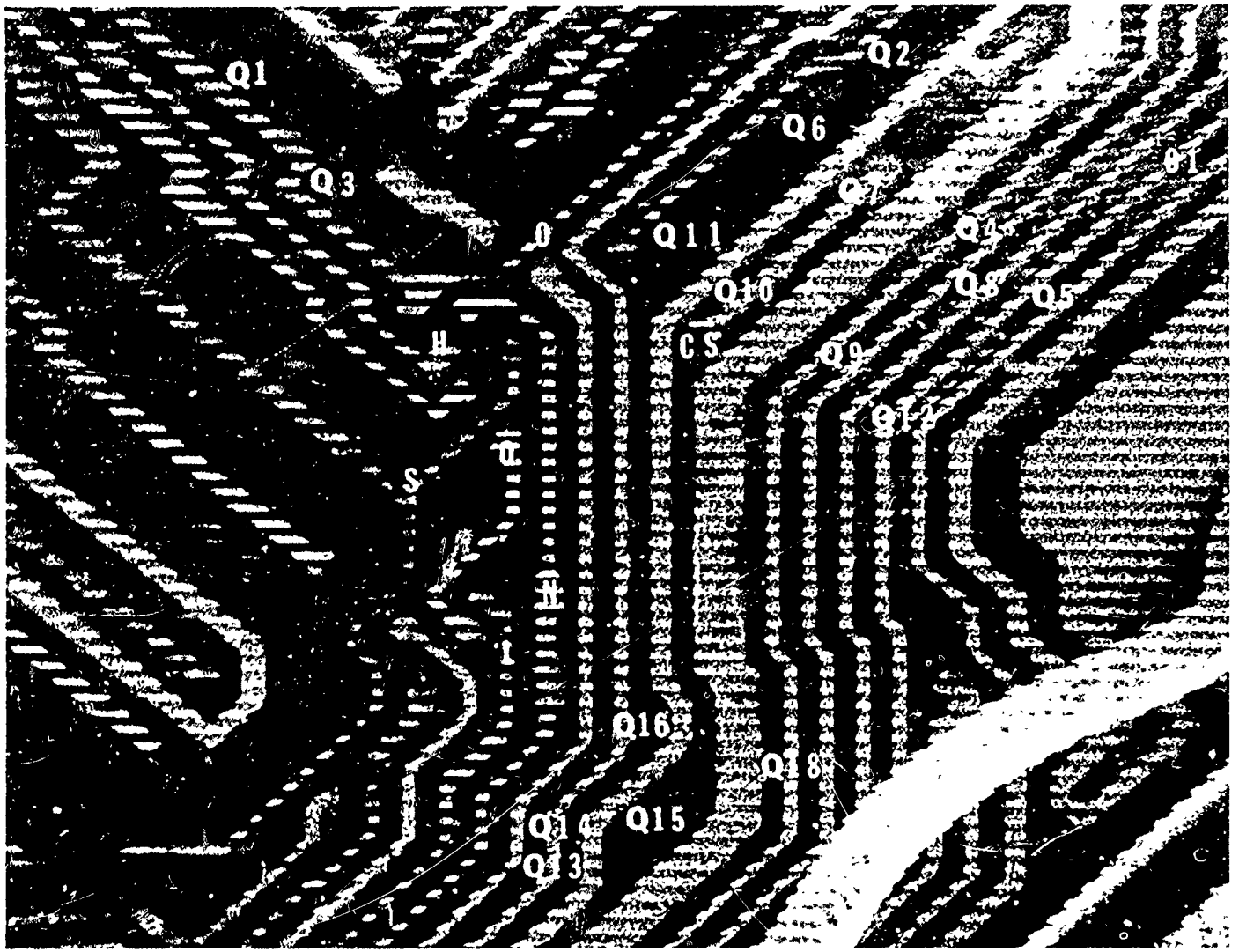

Photo 6-42 Voltage Contrast Micrograph of the Sense Amp Control Circuit. 1.3 KV, Mag. - 390X

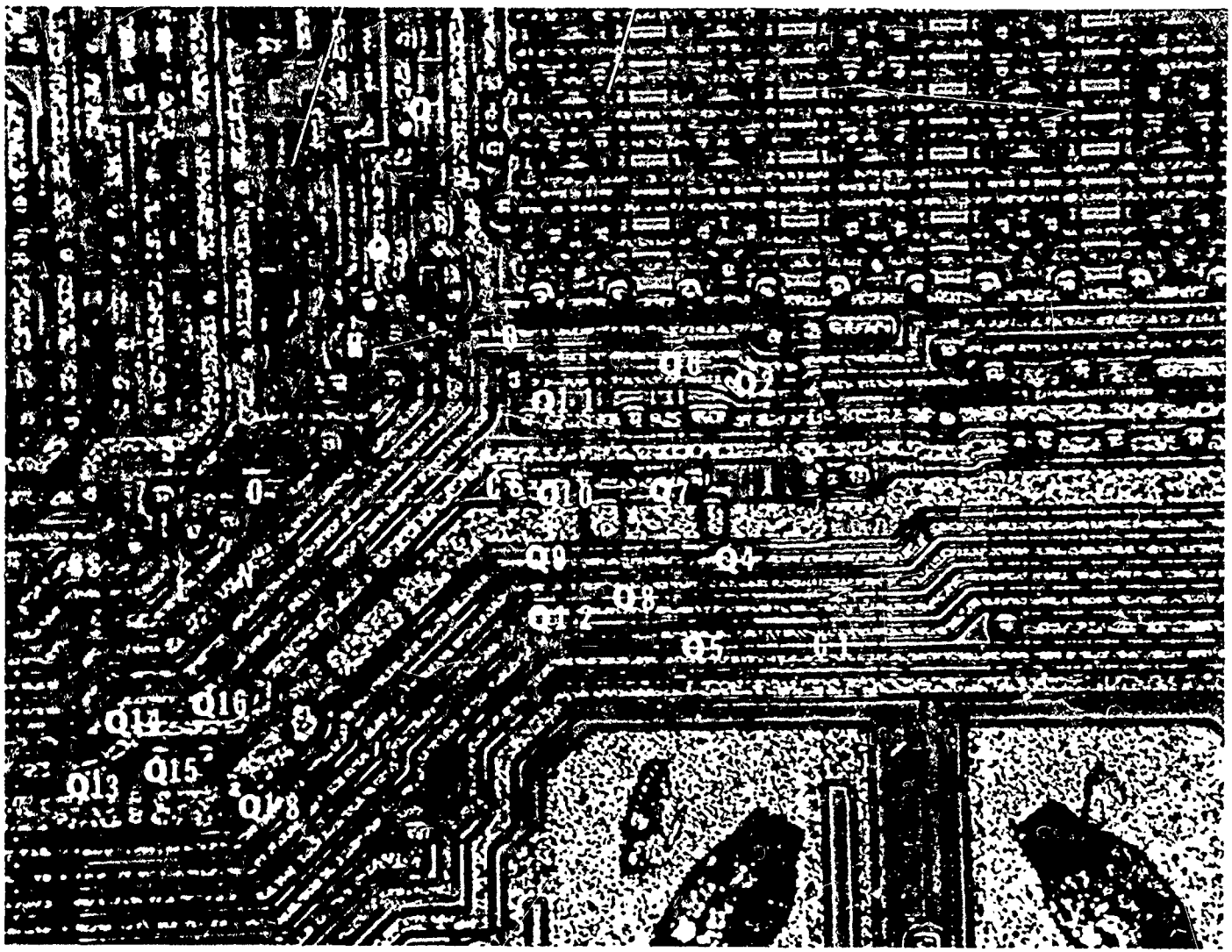

Photo 6-43 Light Photograph of the Sense Amp Control Circuit. Mag. - 300X

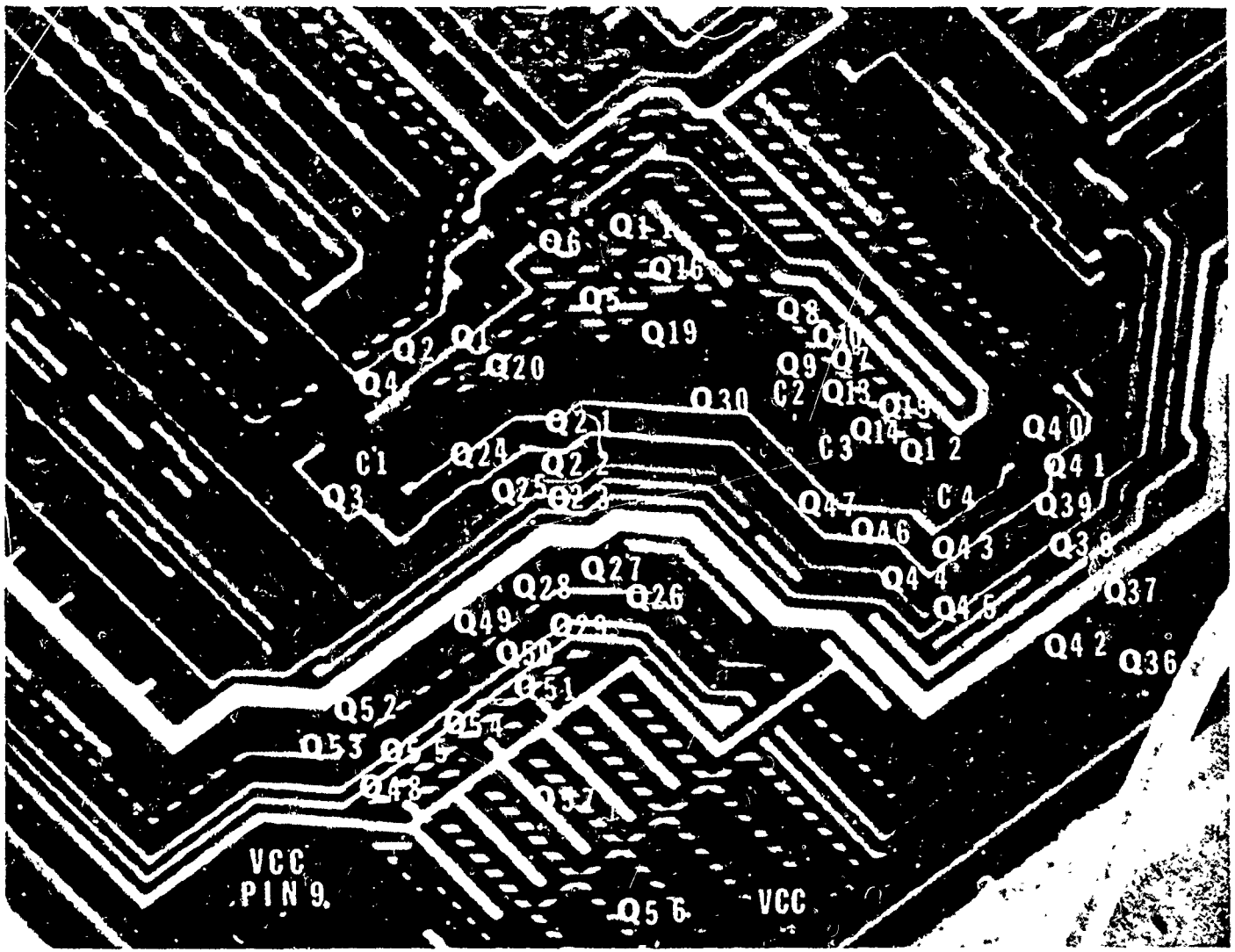

Photo 6-44 Voltage Contrast Micrograph of the Data Output Buffer/Latch. 1.3 KV, Mag. - 180X

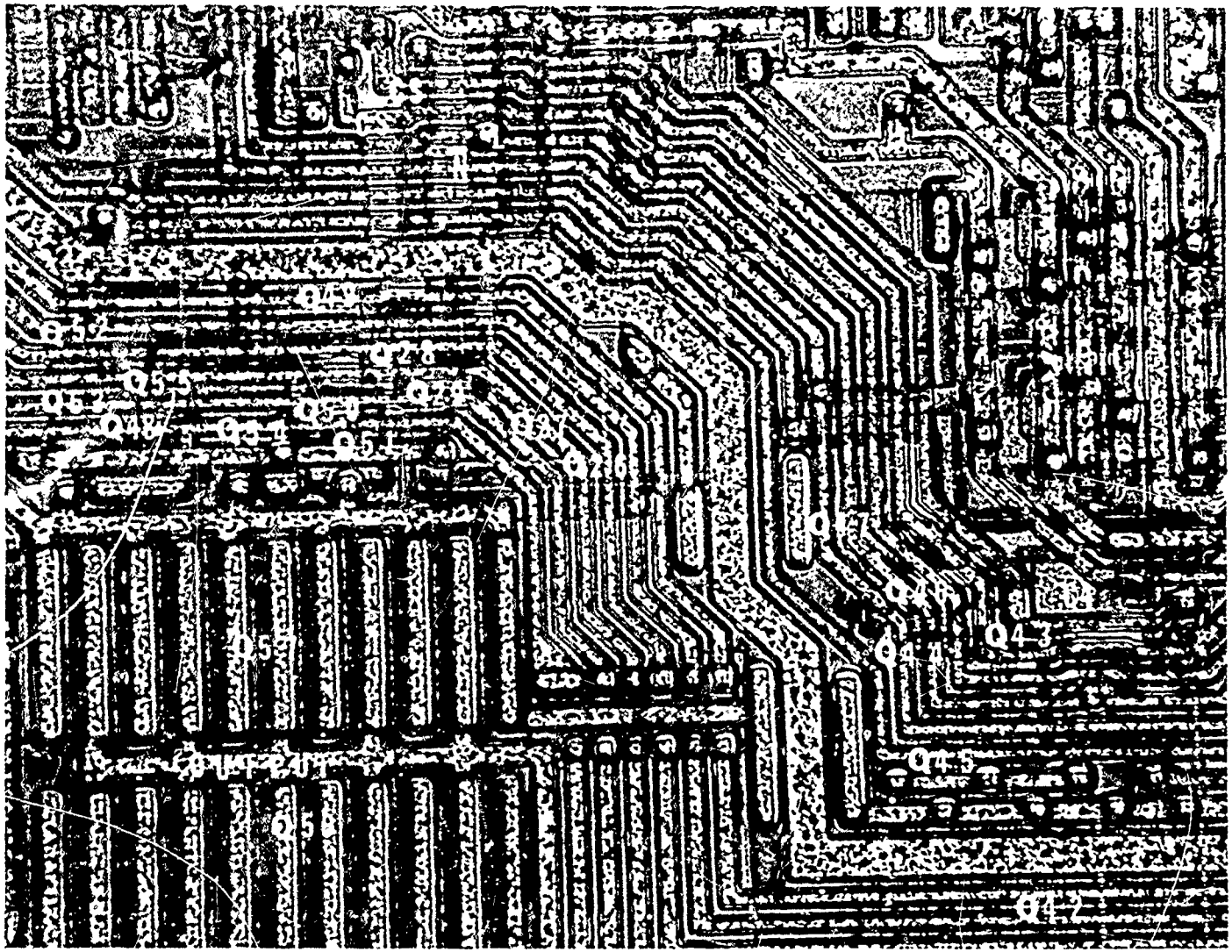

Photo 6-45 One of Three Light Photographs of the Data Output Buffer/Latch. Mag. - 300X

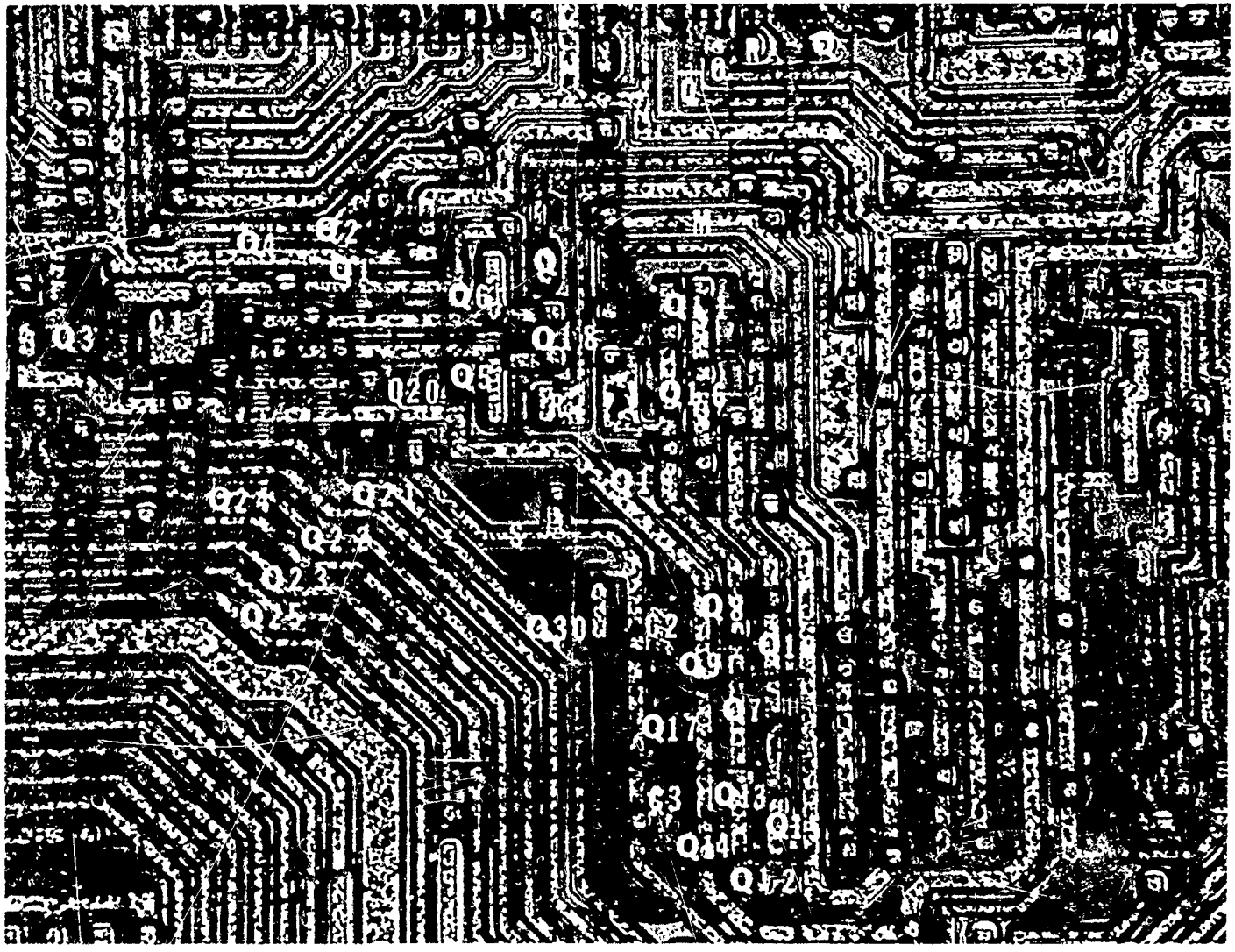

Photo 6-46 Two of Three Light Photographs of the Data Output Buffer/Latch. Mag. - 300X

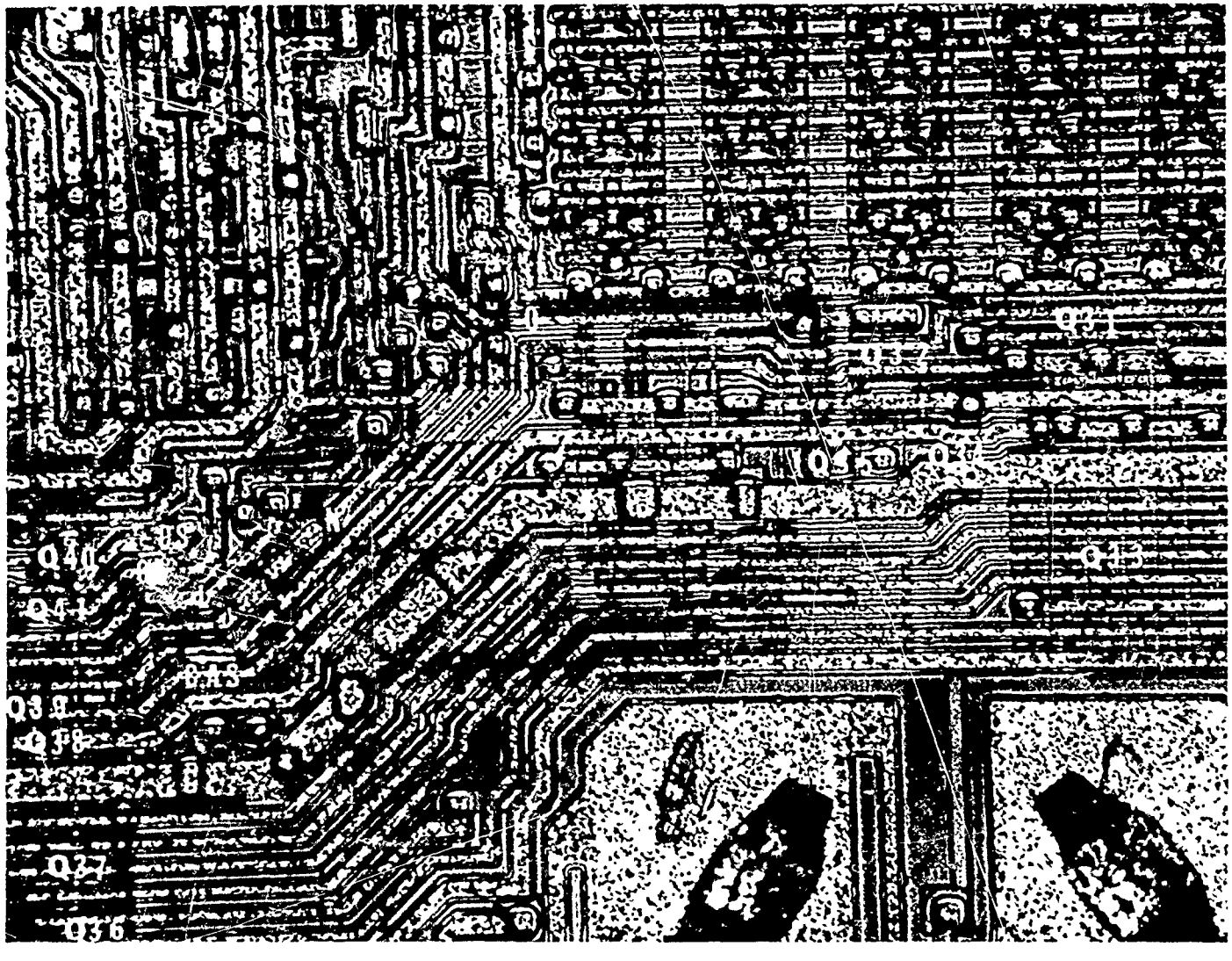

Photo 6-47 Three of Three Light Photographs of the Data Output Buffer/Latch. Mag. - 300X

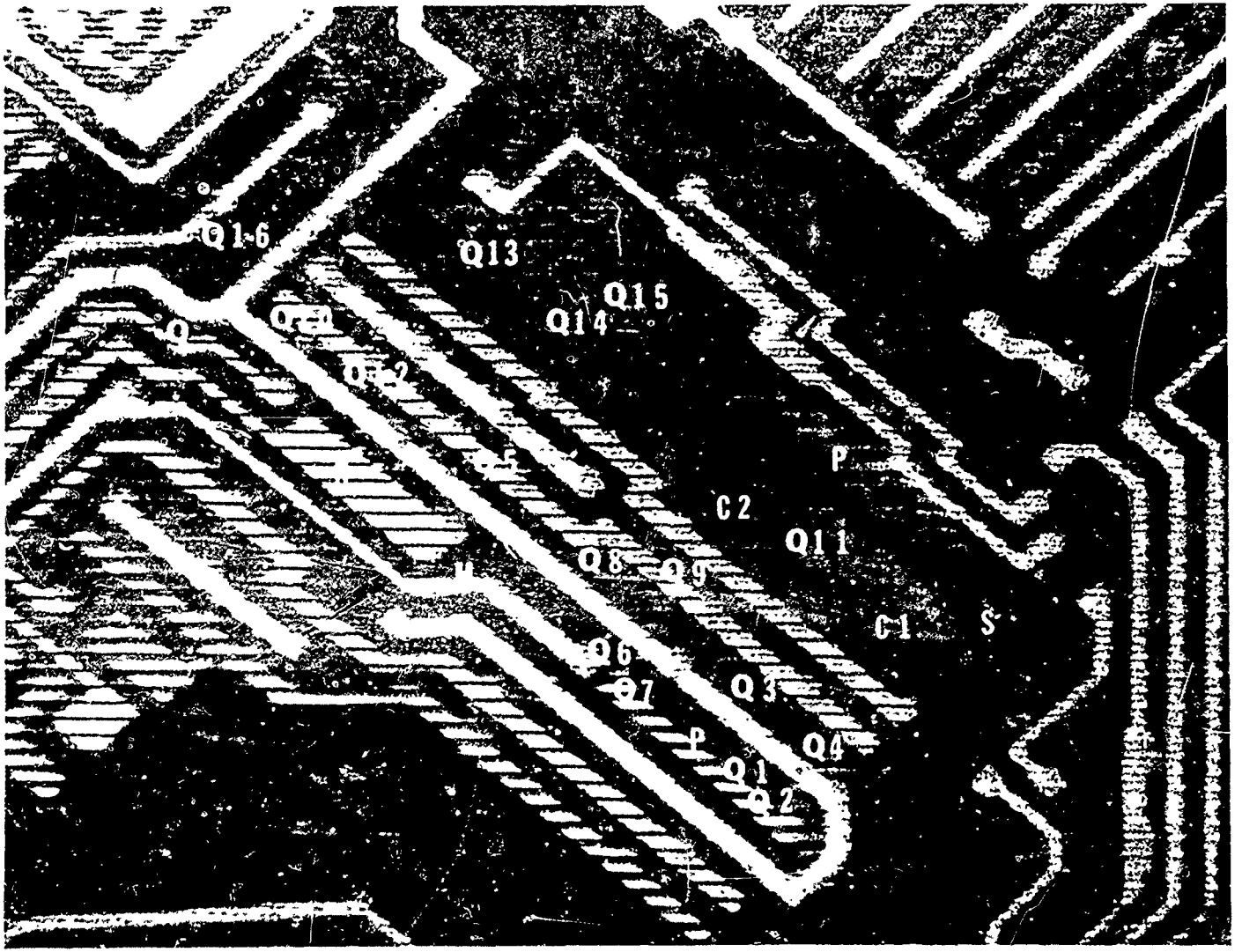

Photo 6-48 Voltage Contrast Micrograph of the Sense Amp Latch Circuit. 1.3 KV, Mag. - 500X

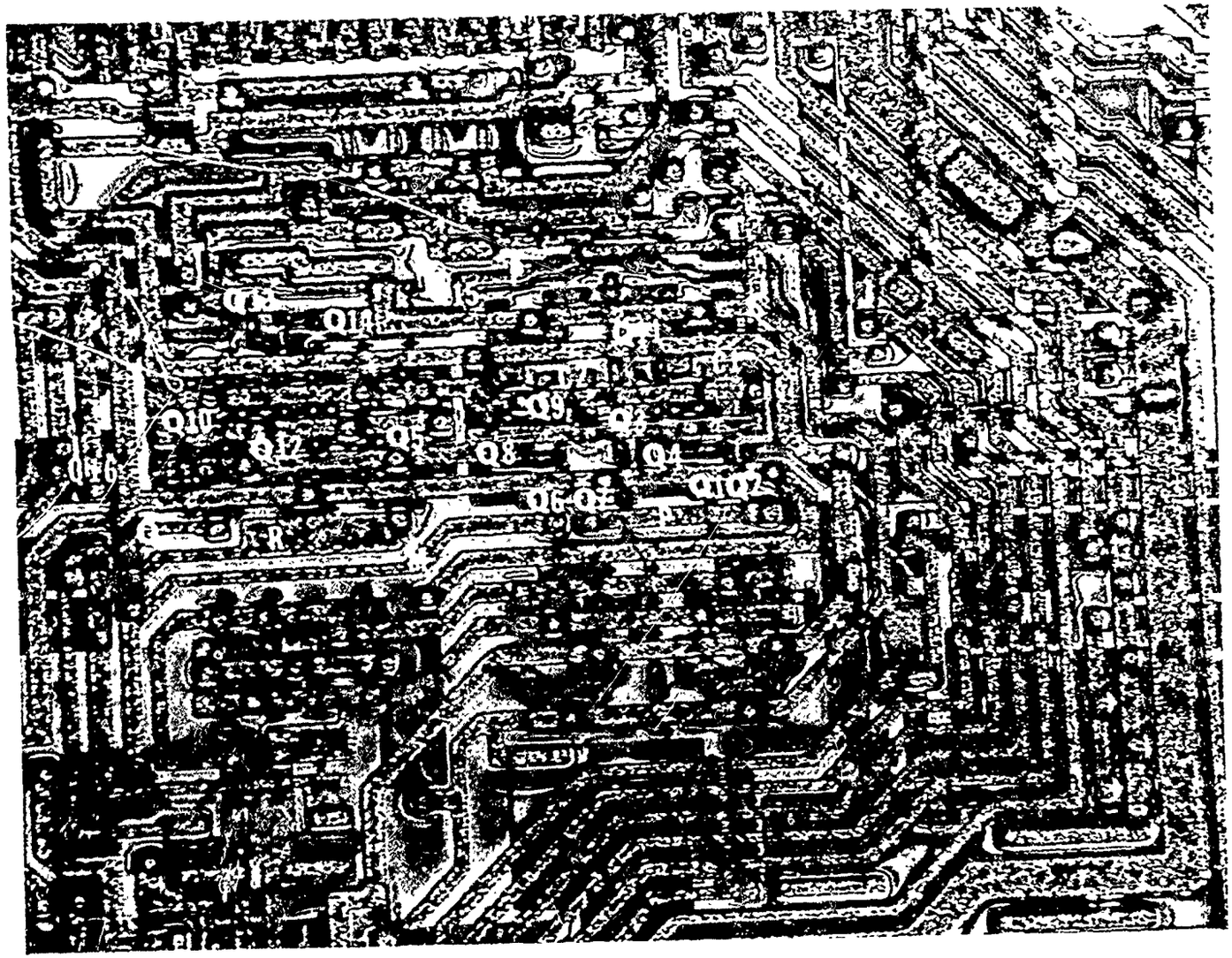

Photo 6-49 Light Photograph of the Sense Amp Latch Circuit. Mag. - 300X

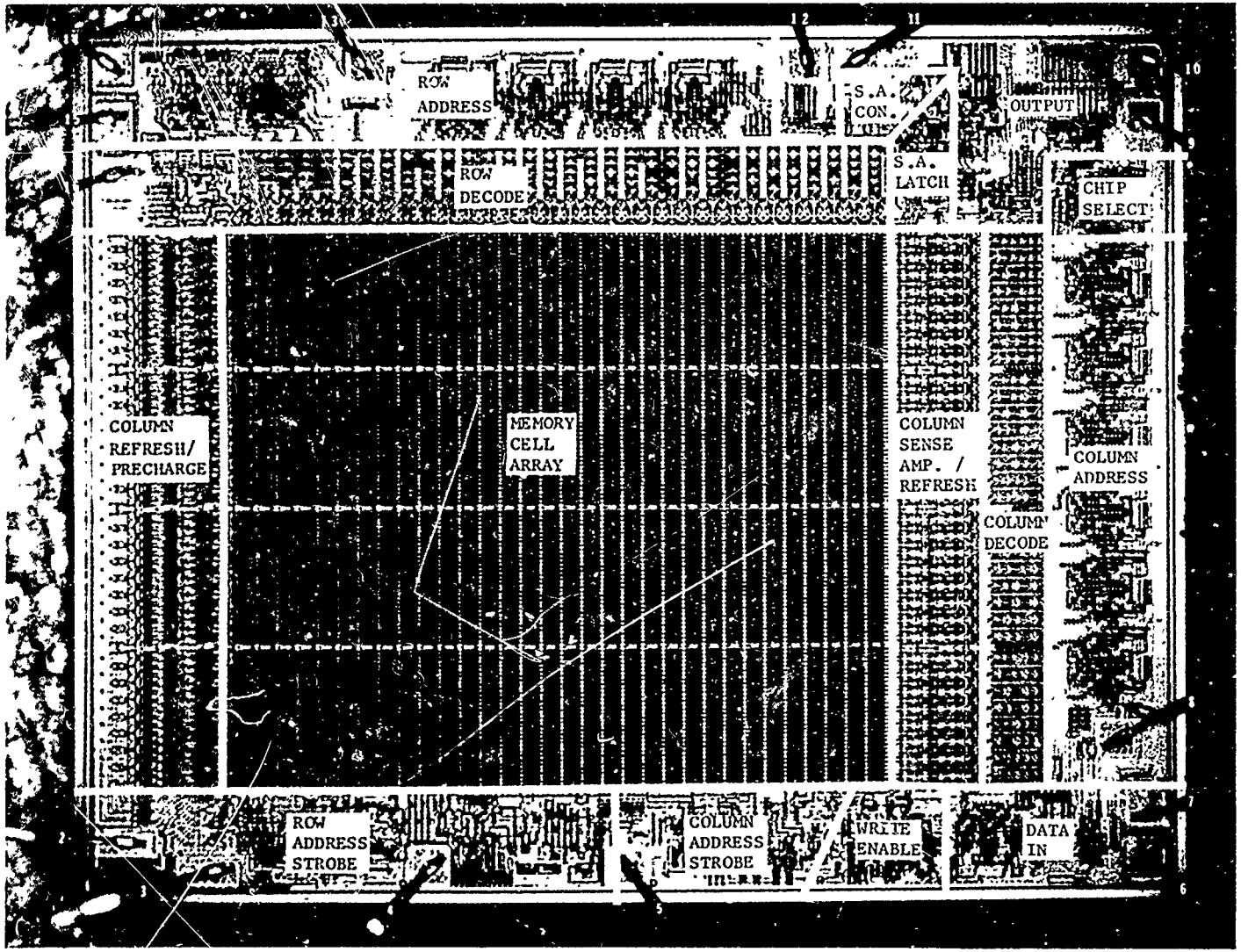

Photo 6-50 Light Photograph Showing the Chip Organization. Mag. - 40X

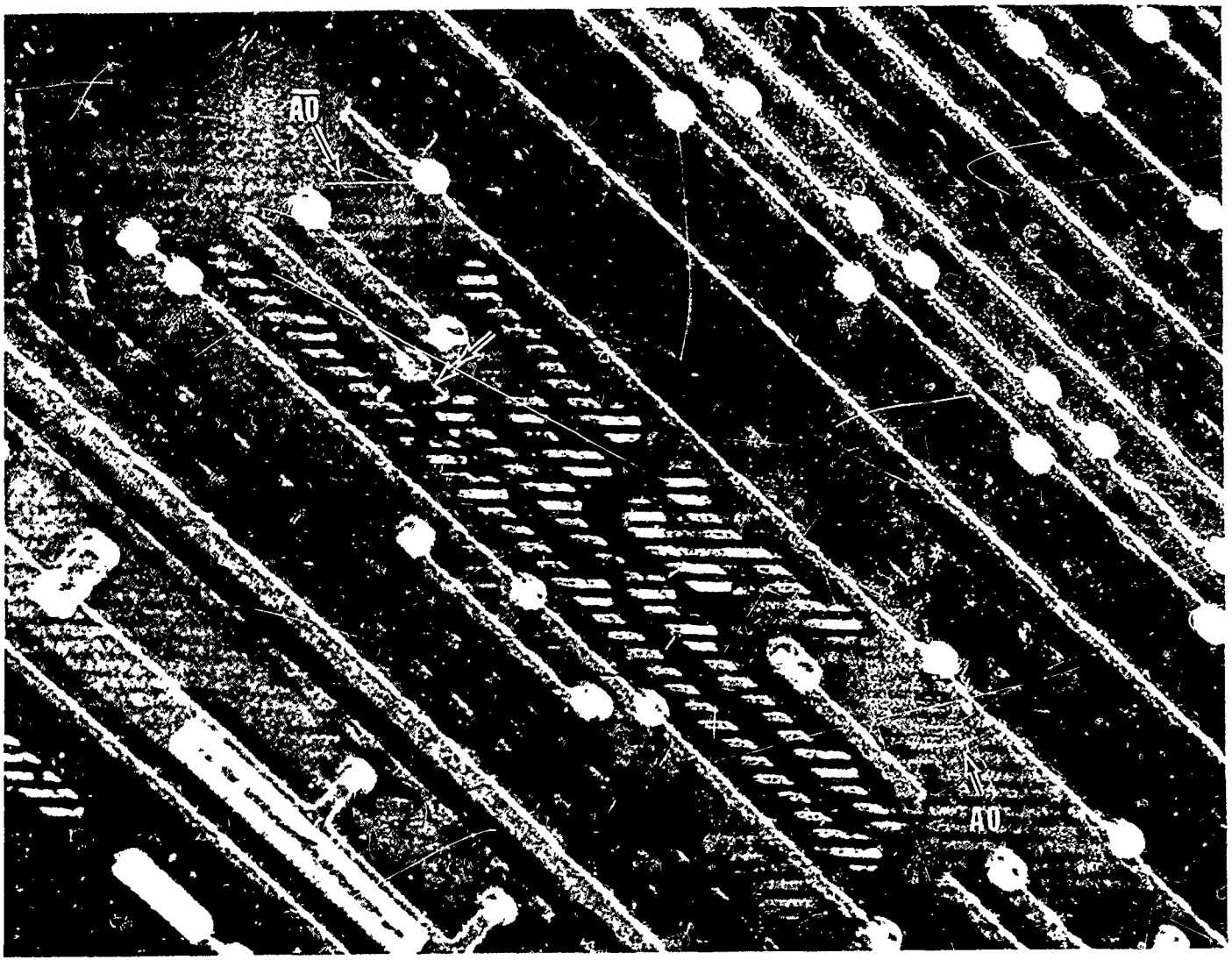

Photo 6-51 Voltage Contrast Micrograph Showing the Failure Isolation in the AO Column Address Circuit. The Arrow at AO Shows a Typical Output Response. Arrow at AO-NOT Shows no Output. Double Arrow Locates Open. 1.3 KV, Mag. - 550X

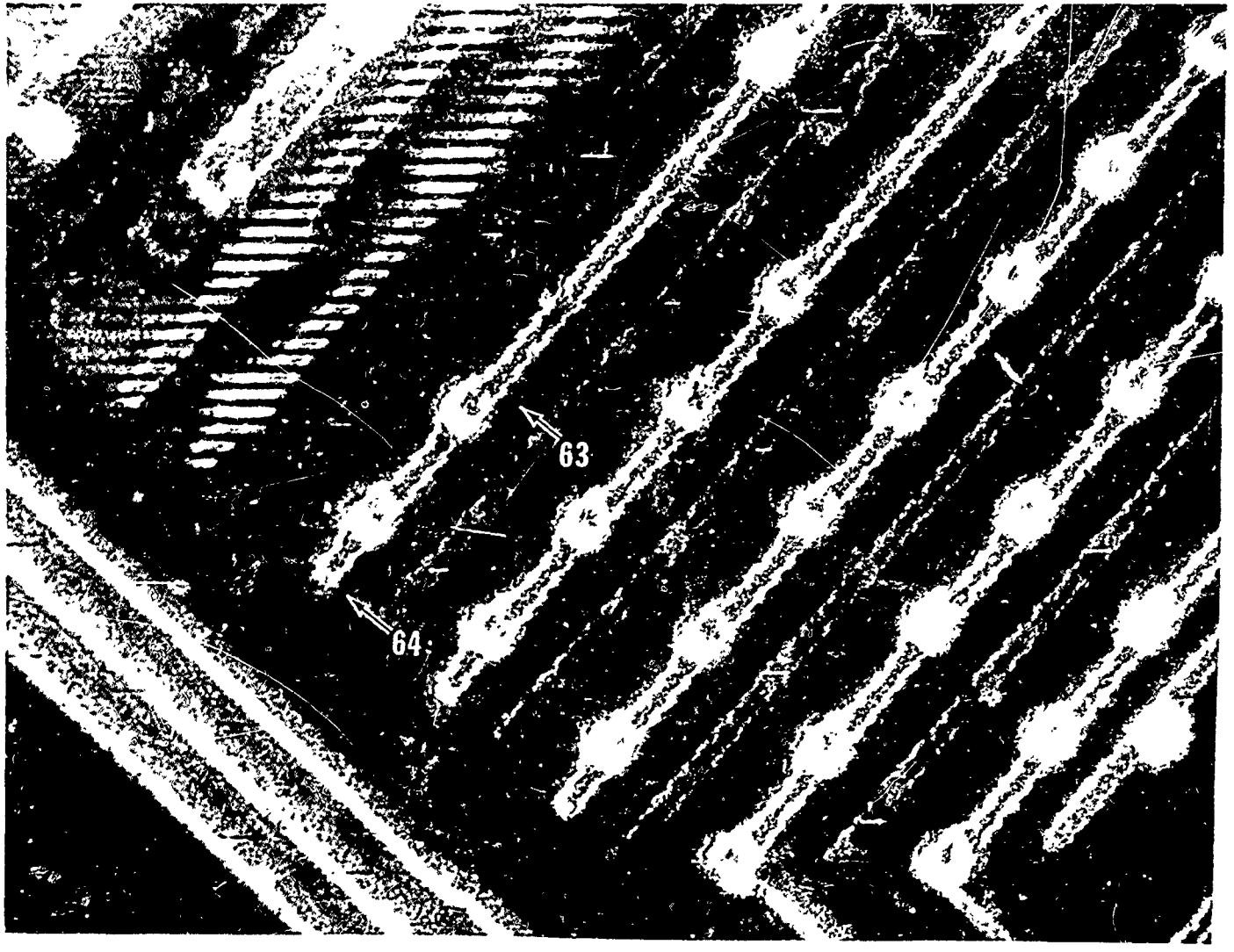

Photo 6-52 Voltage Contrast Micrograph of the Column Decode Circuit Showing no Access Enable from 63 and 64 (Arrows). The V_{SS} Open is Located at the Arrow. 1.3 KV, Mag. - 850X

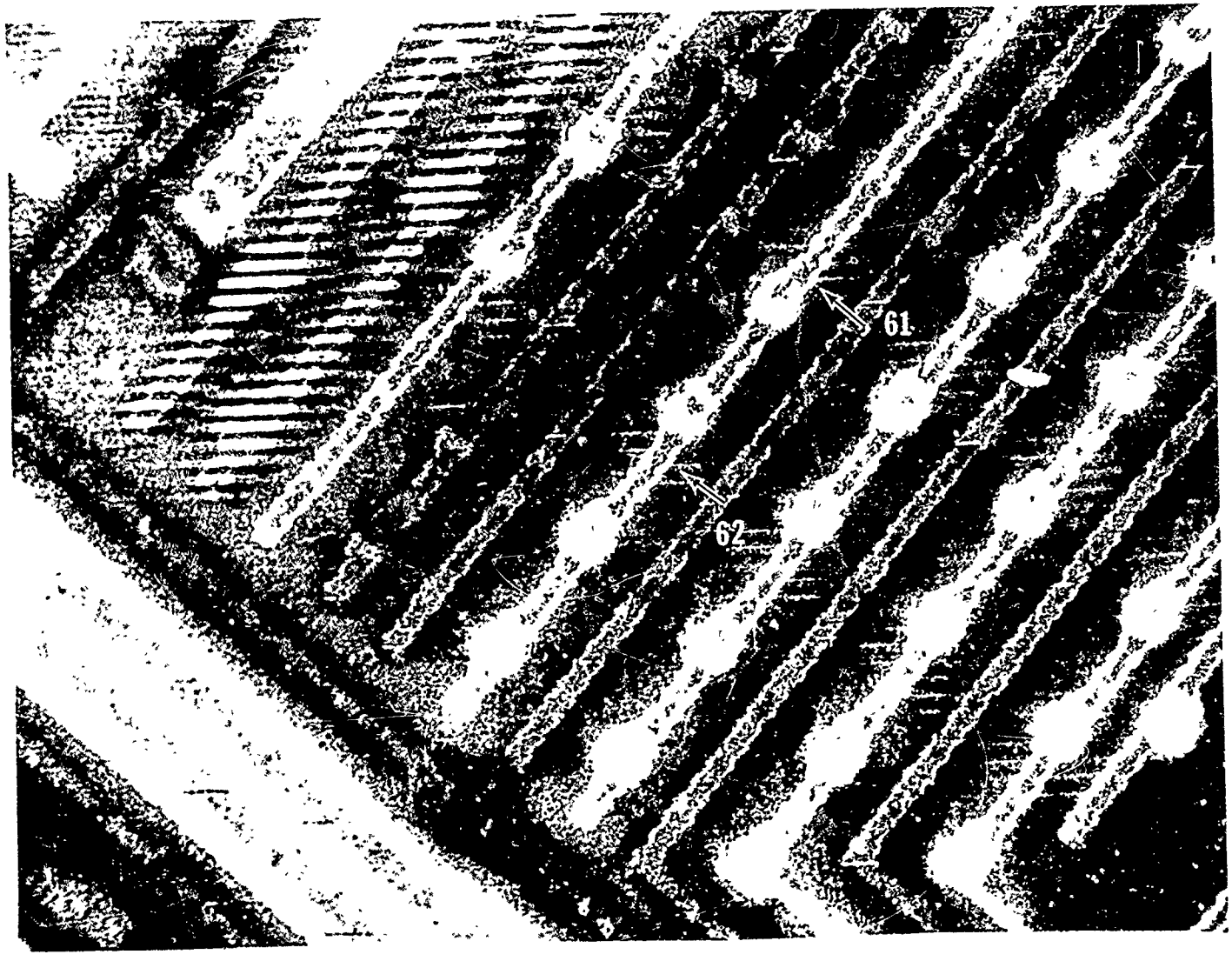

Photo 6-53 Voltage Contrast Micrograph of the Column Decode Circuit Showing a Typical Access Enable from 61 and 62. 1.3 KV, Mag. - 850X

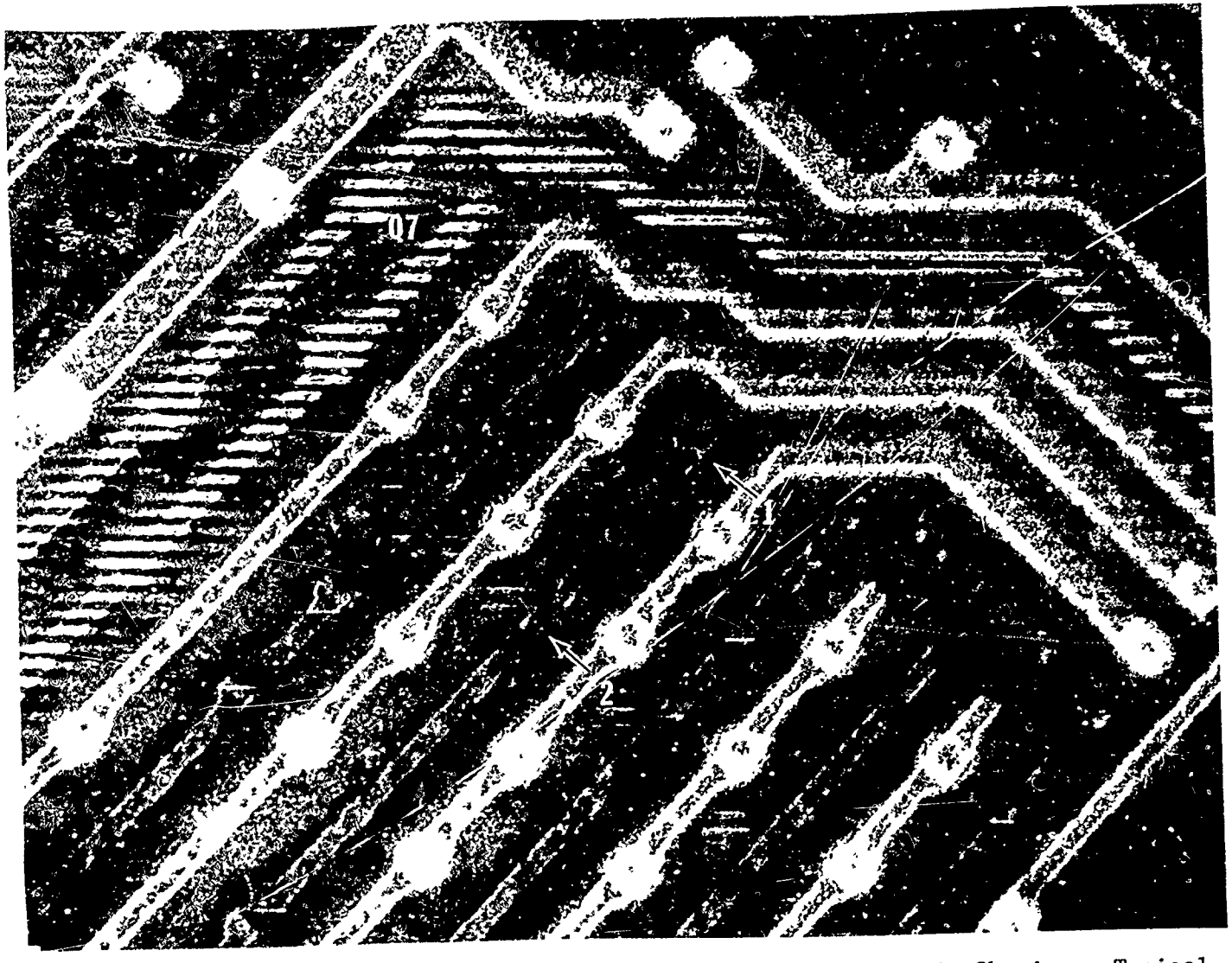

Photo 6-54 Voltage Contrast Micrograph of the Column Decode Circuit Showing a Typical Access Enable from Decode 2 and no Response from Decode 1. 1.3 KV, Mag. - 860X

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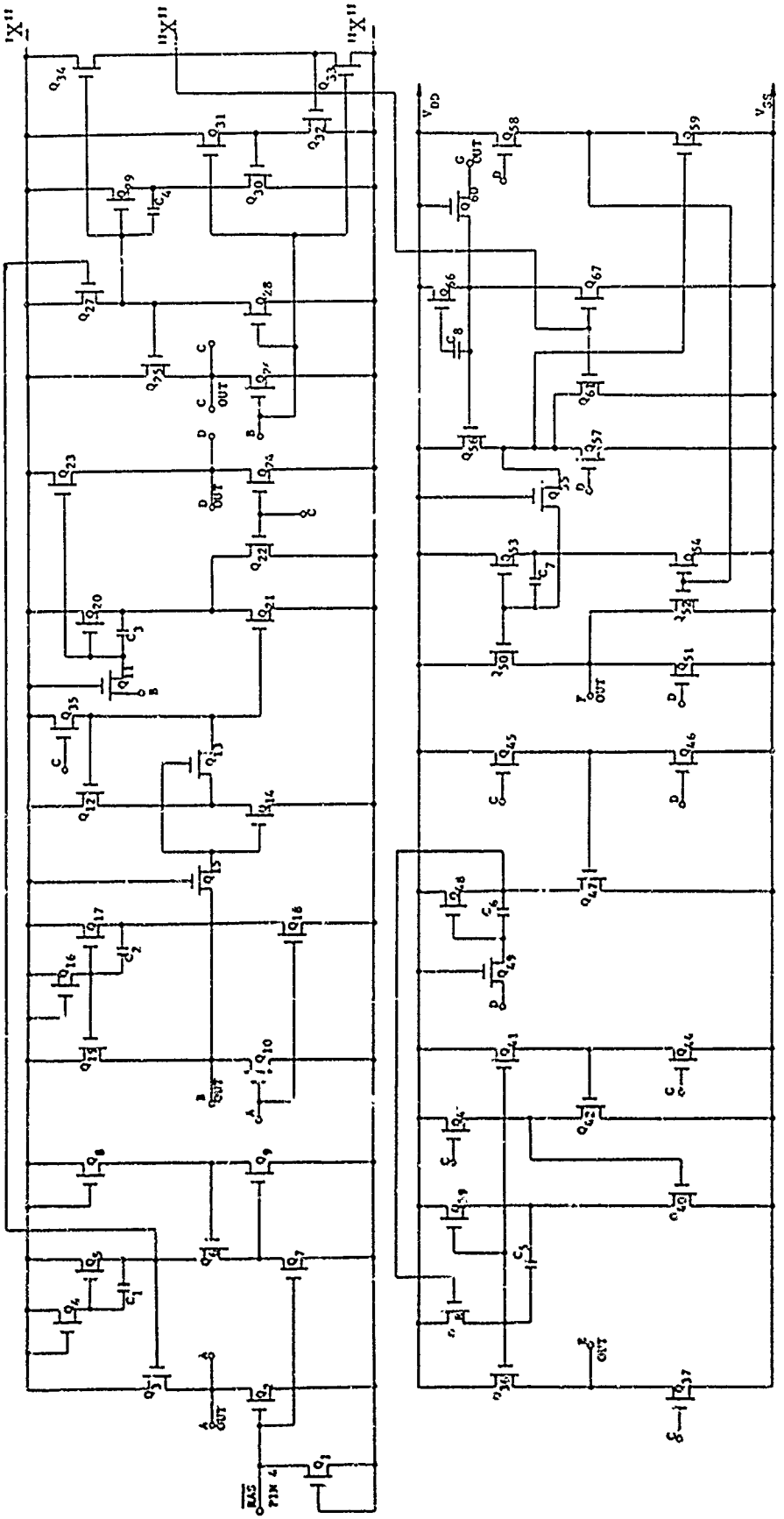


Figure 6-1 Schematic, Row Address Strobe. (concluded next page)

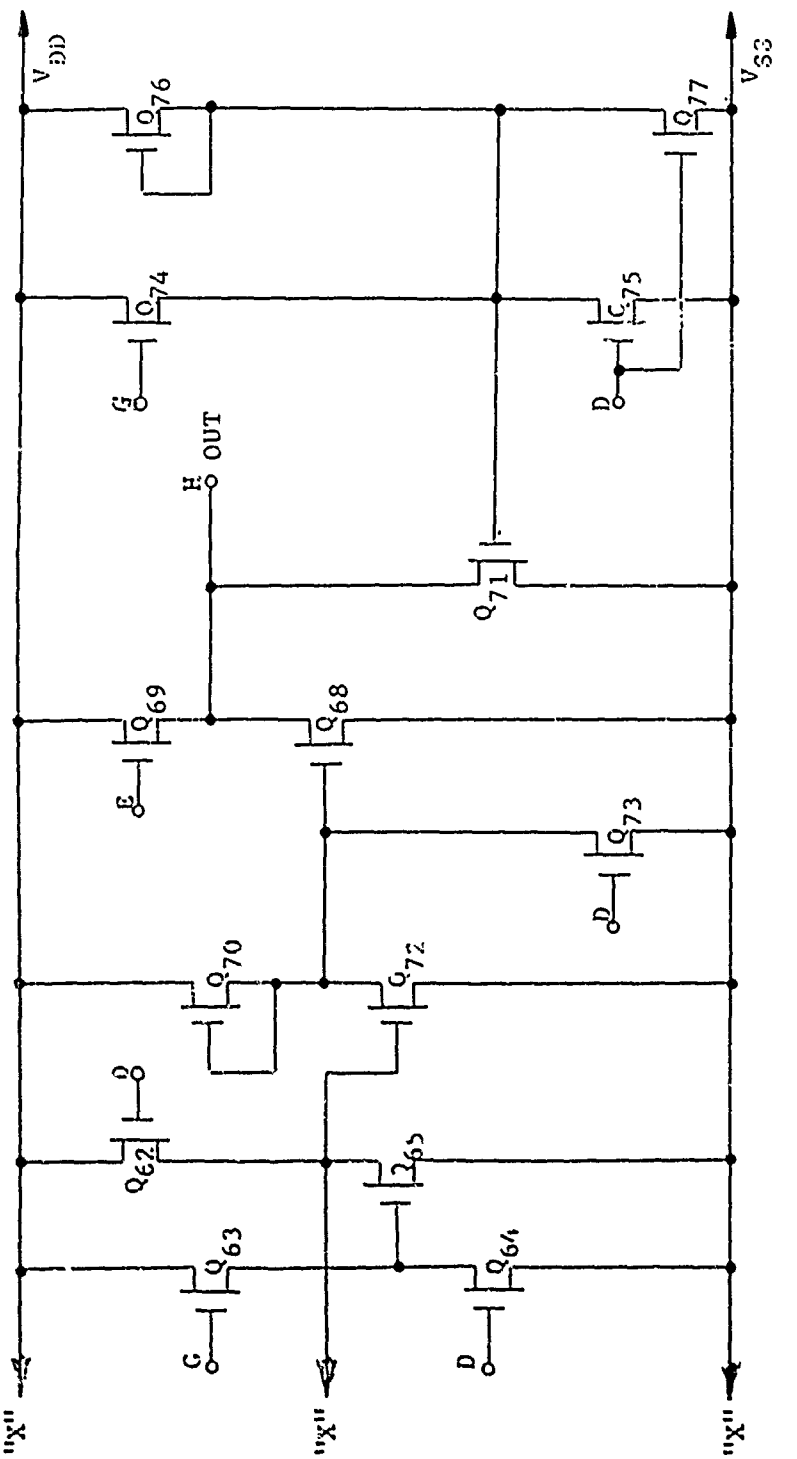
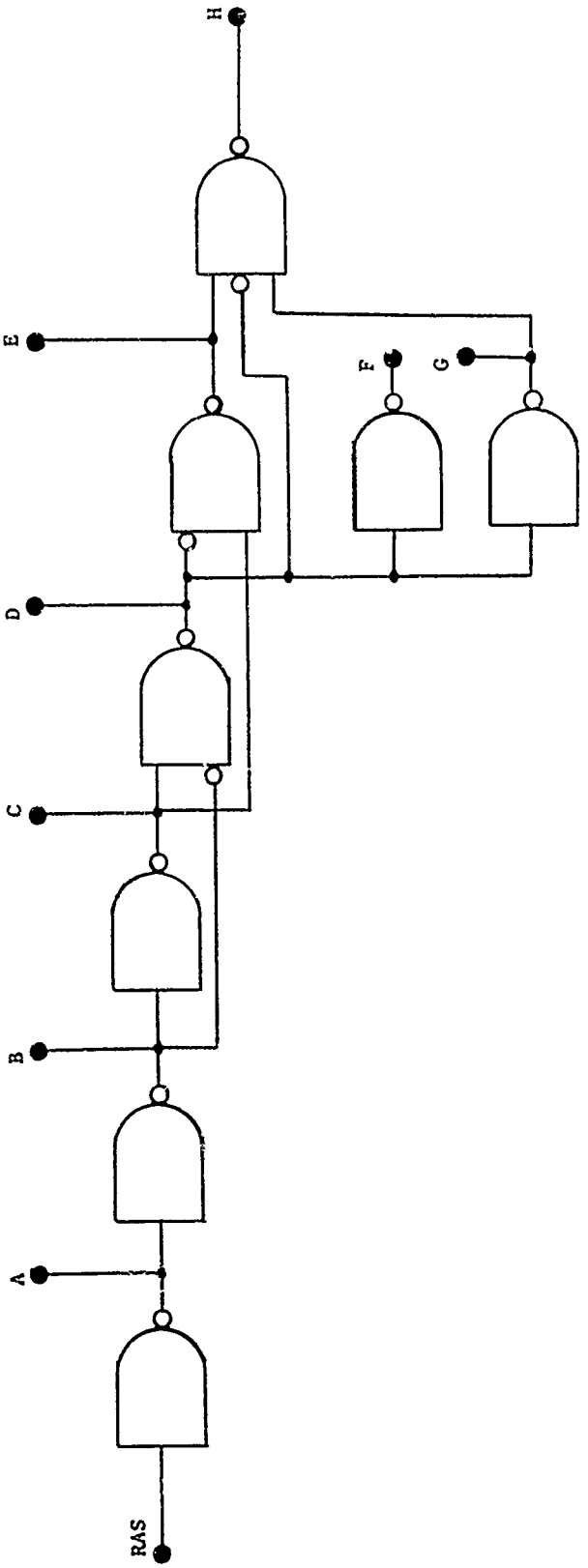


Figure 6-1 Schematic, Row Address Strobe. (concluded)



RAS	A	B	C	D	E	F	G	H
H	L	H	L	H	H	L	L	H
L	H	L	H	L	L	H	H	L

Figure 6-2 Logic Diagram, Row Addrss Strobe (RAS)

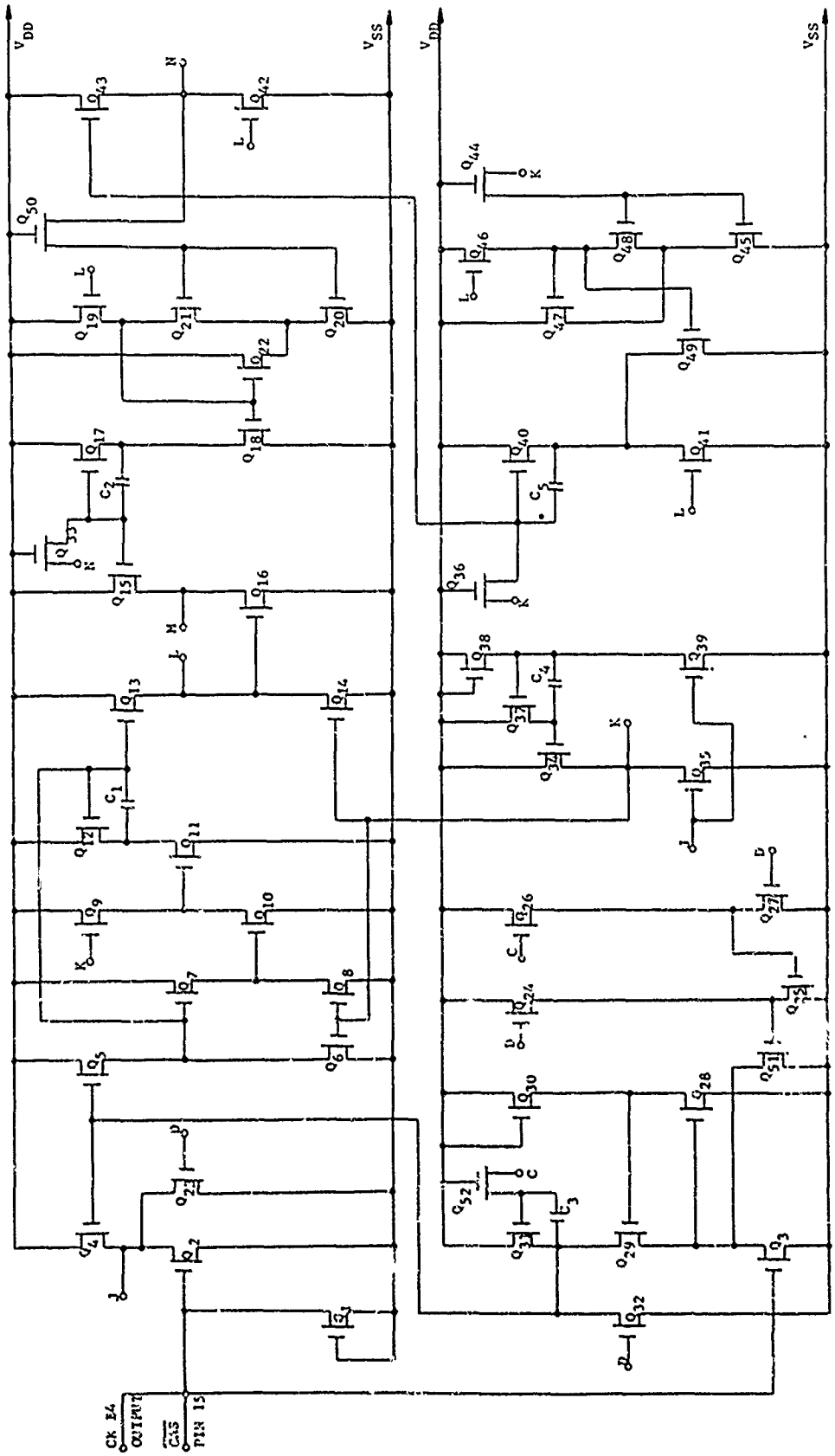
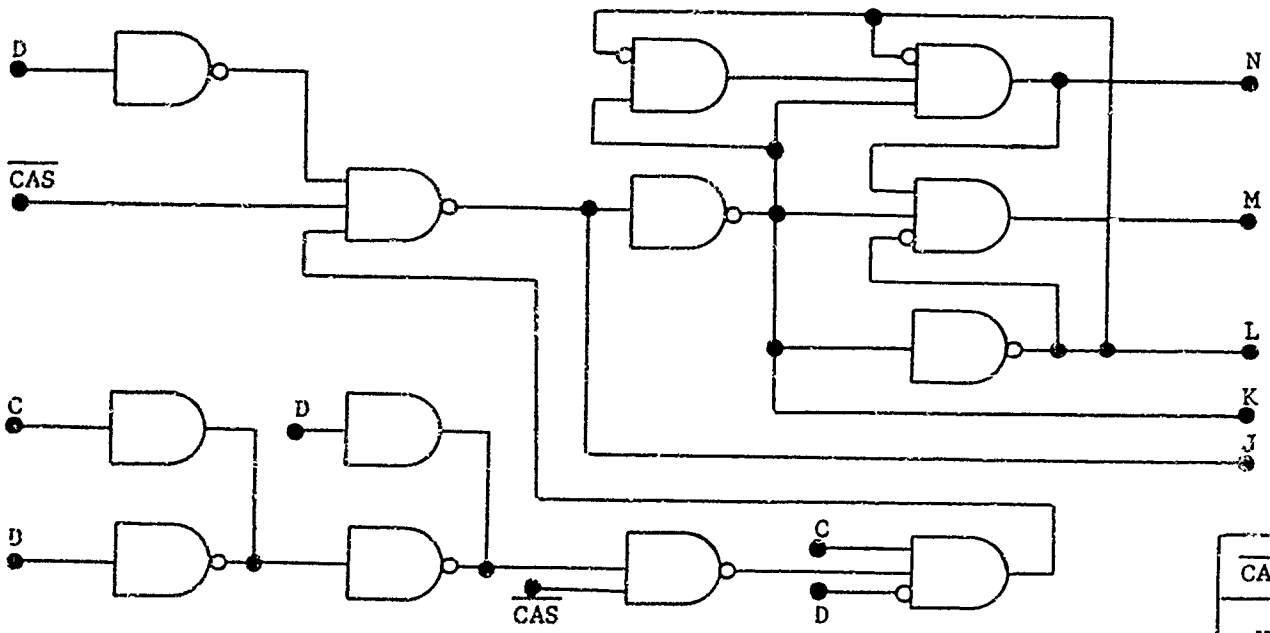


Figure 6-3 Schematic, Column Address Strobe(CAS)



$\overline{CAS}$	J	K	L	M	N
H	L	H	L	H	H
L	H	L	H	L	L

ASSUME $\overline{RAS}$ = L

$\therefore$ C = H, D = L

420

Figure 6-4 Logic Diagram, Column Address Strobe (CAS)

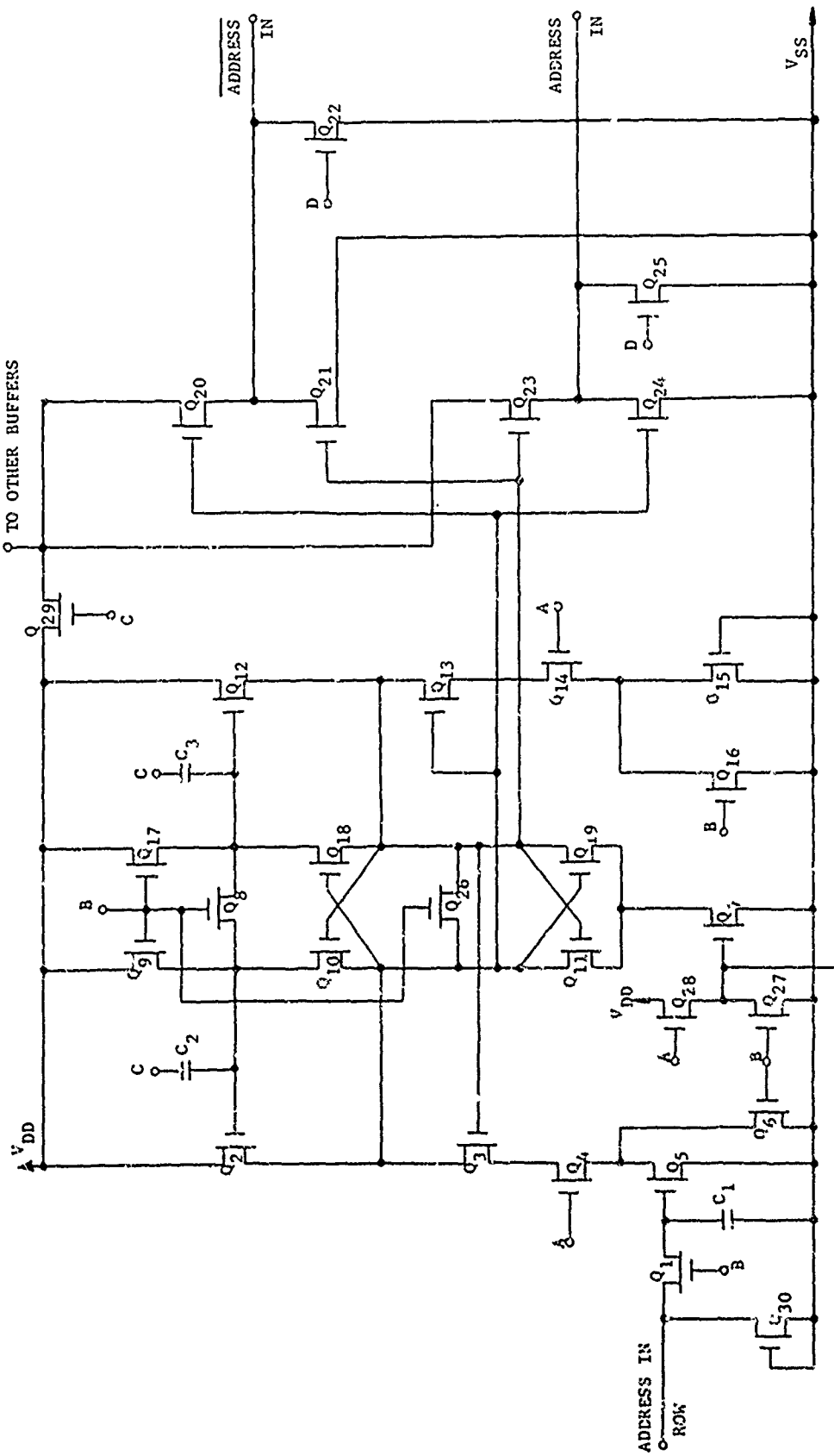


Figure 6-5 Schematic, Row Address Buffer

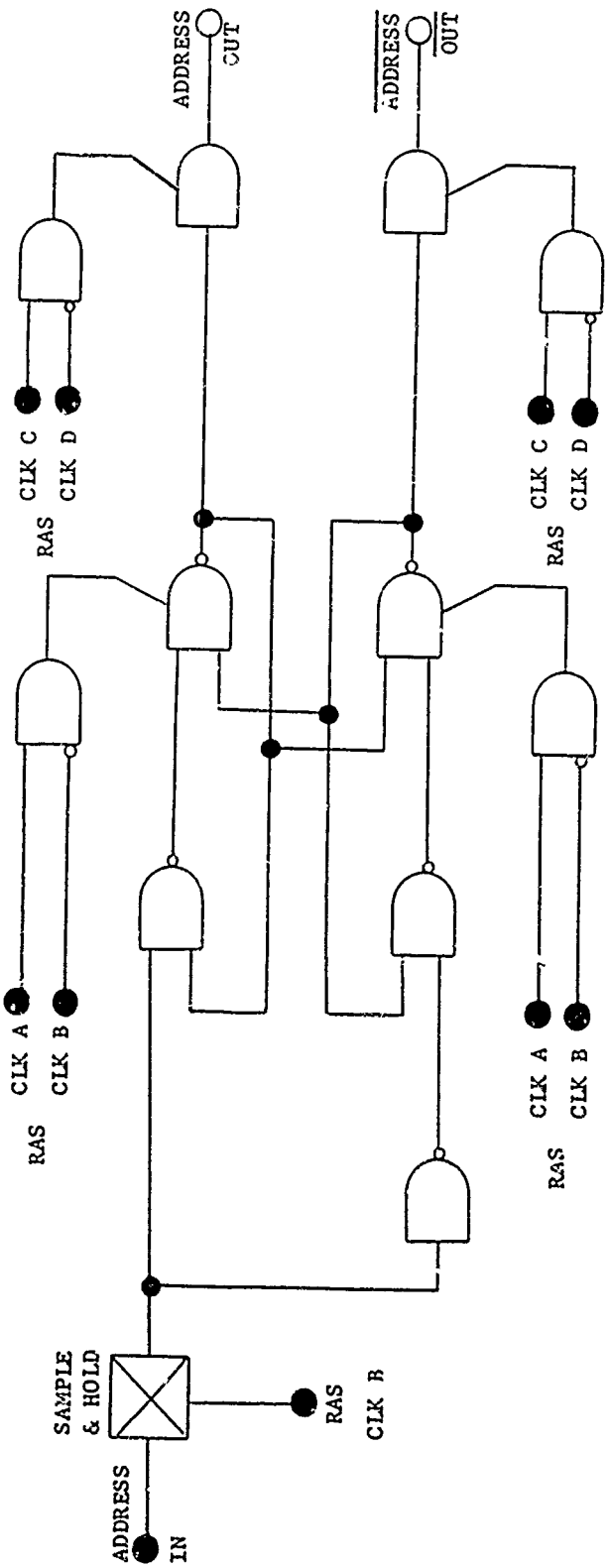


Figure 6-6 Logic Diagram, Row Address Buffer

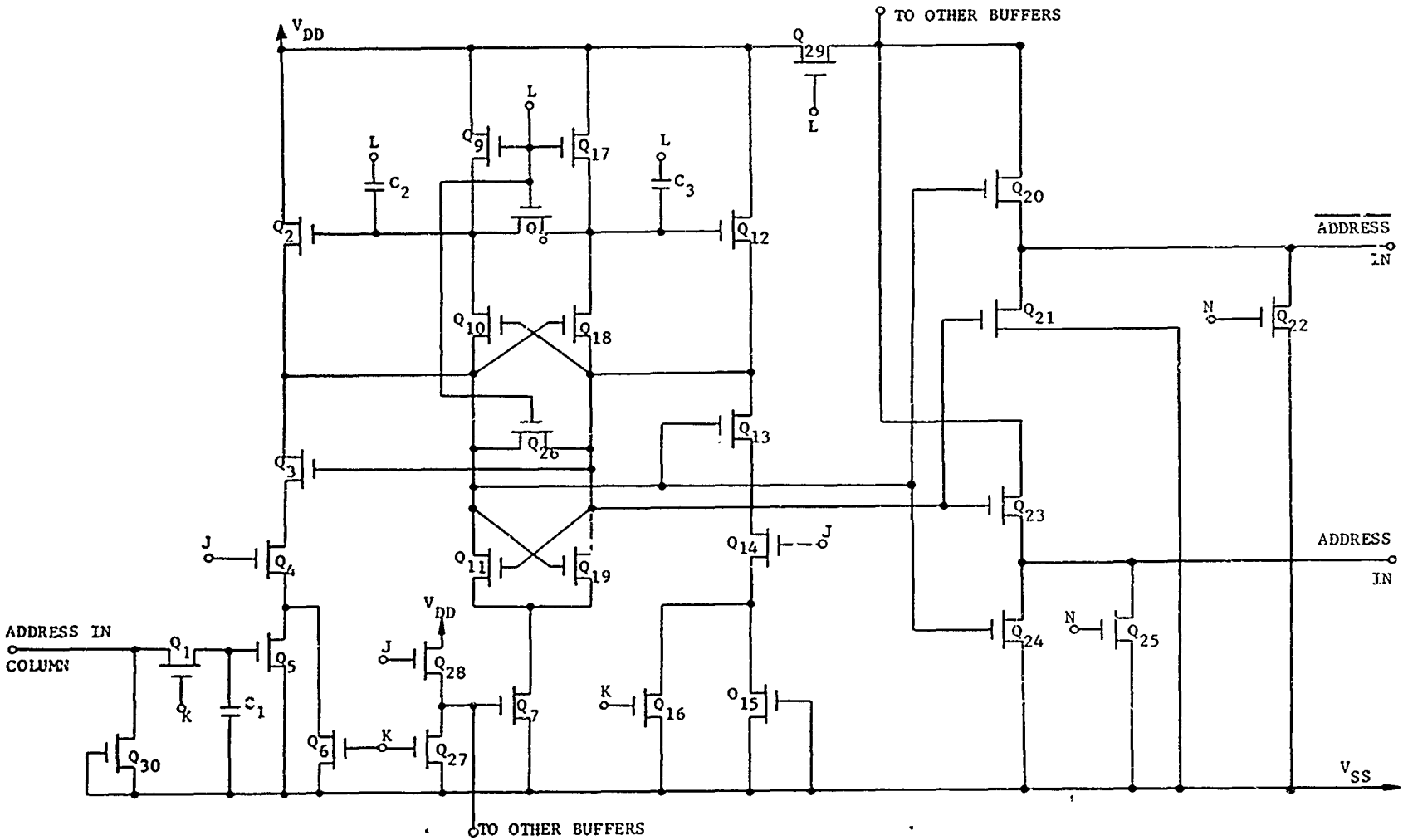


Figure 6-7 Schematic, Column Address Buffer

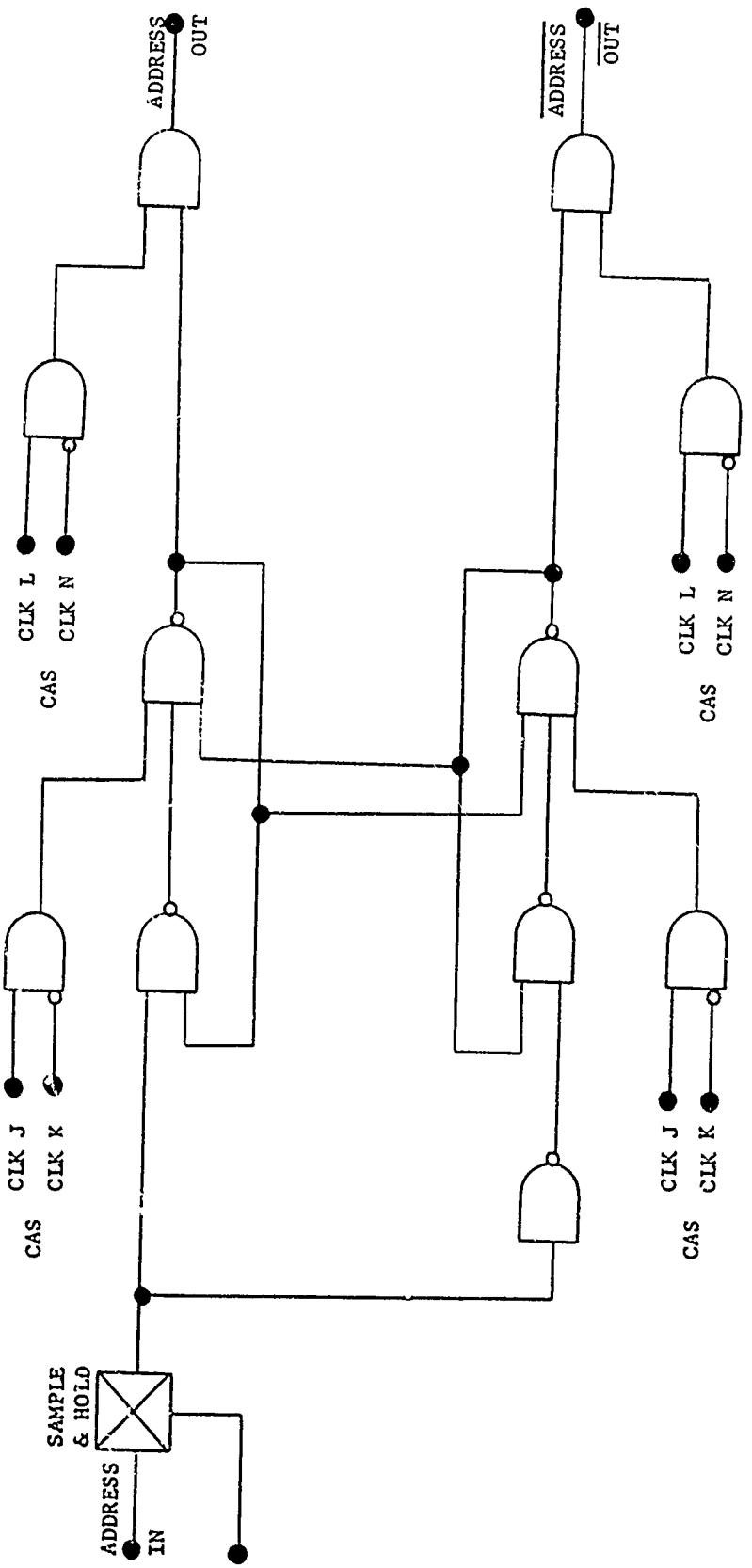


Figure 6-8 Logic Diagram, Column Address Buffer

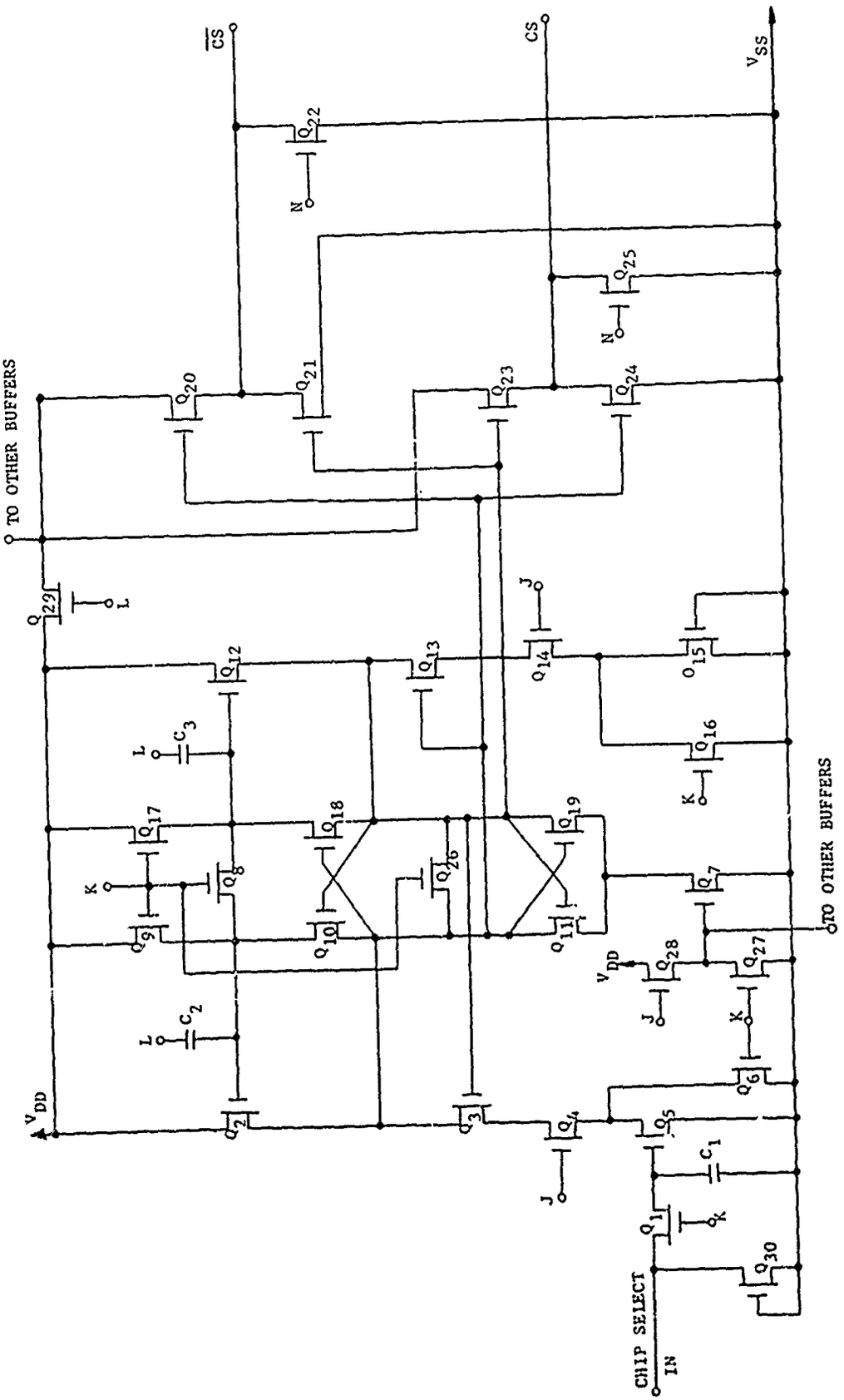


Figure 6-9 Schematic, Chip Select Buffer

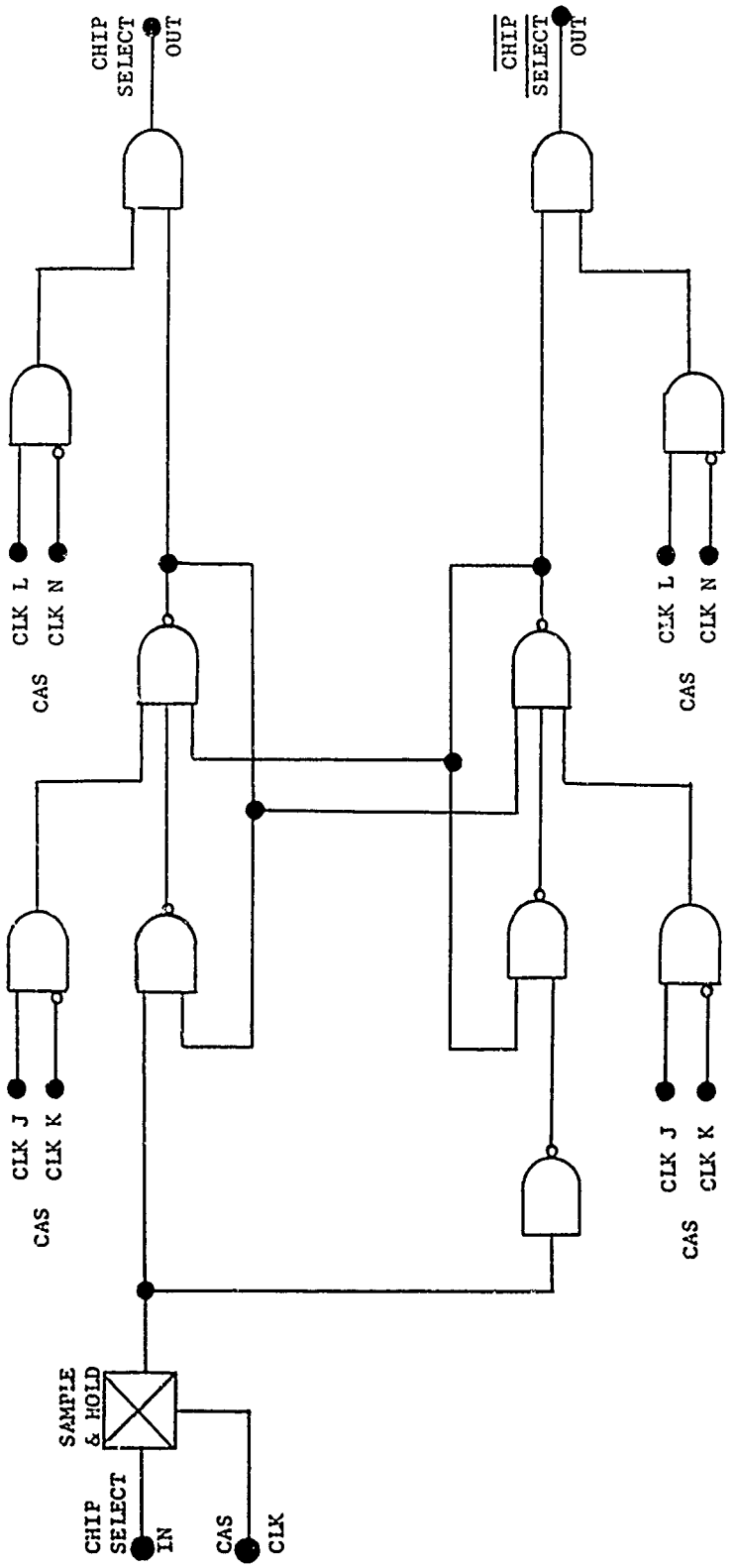


Figure 6-10 Logic Diagram, Chip Select Buffer

WE (IN)		WE OUT				DATA OUT	
				(H)			
$\overline{WE}$	CAS	WE	$\overline{WE}$	P	N	R	Q
H	H	L	H	L	H	H	H
H	L	0	0	0	L	0	0
L	H	L	H	L	H	H	H
L	L	H	L	H	L	DI	$\overline{DI}$

NOTE: READ/MODIFY/WRITE MODE
0 = TRISTATE

* ASSUME Q_{21} & Q_{22} ARE DOMINANT, I.E. - IF BOTH ARE "ON" THE OUTPUT IS LOW.

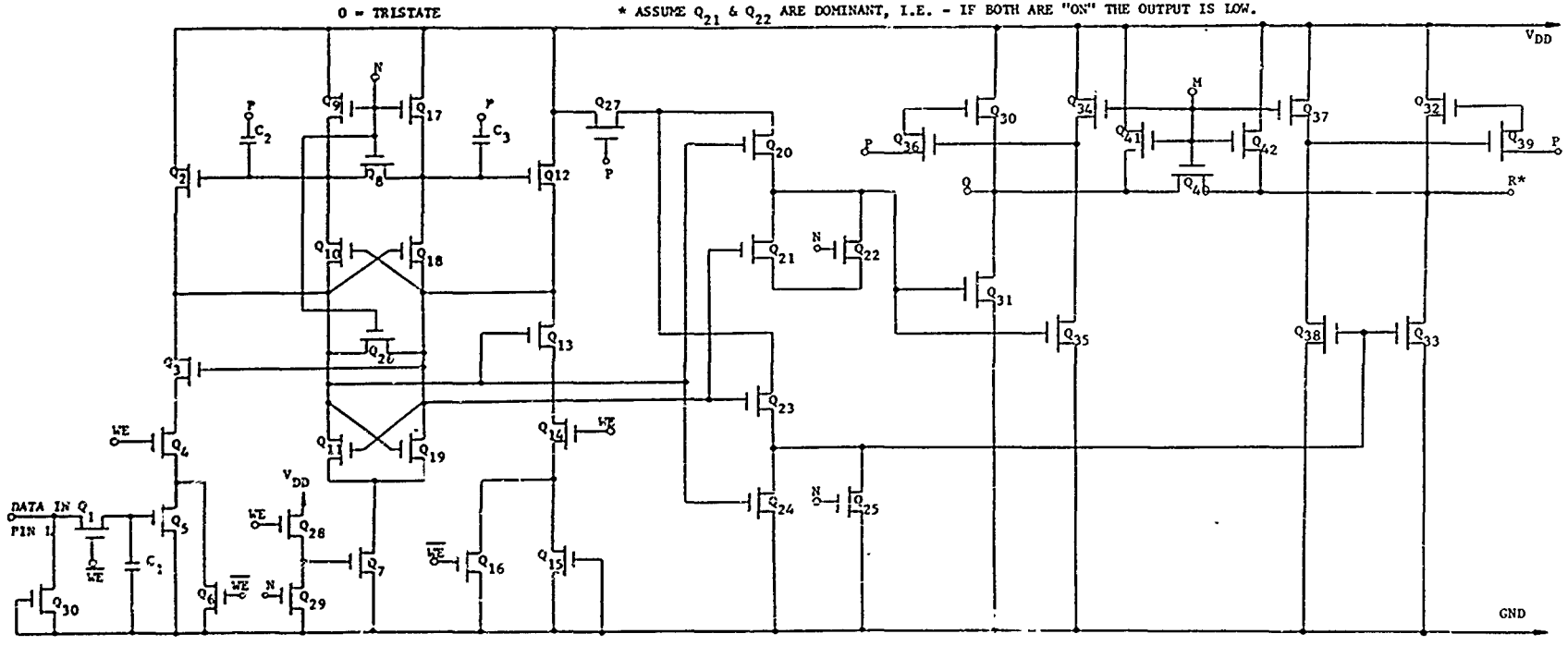


Figure 6-11 Schematic, Data In Buffer/Latch

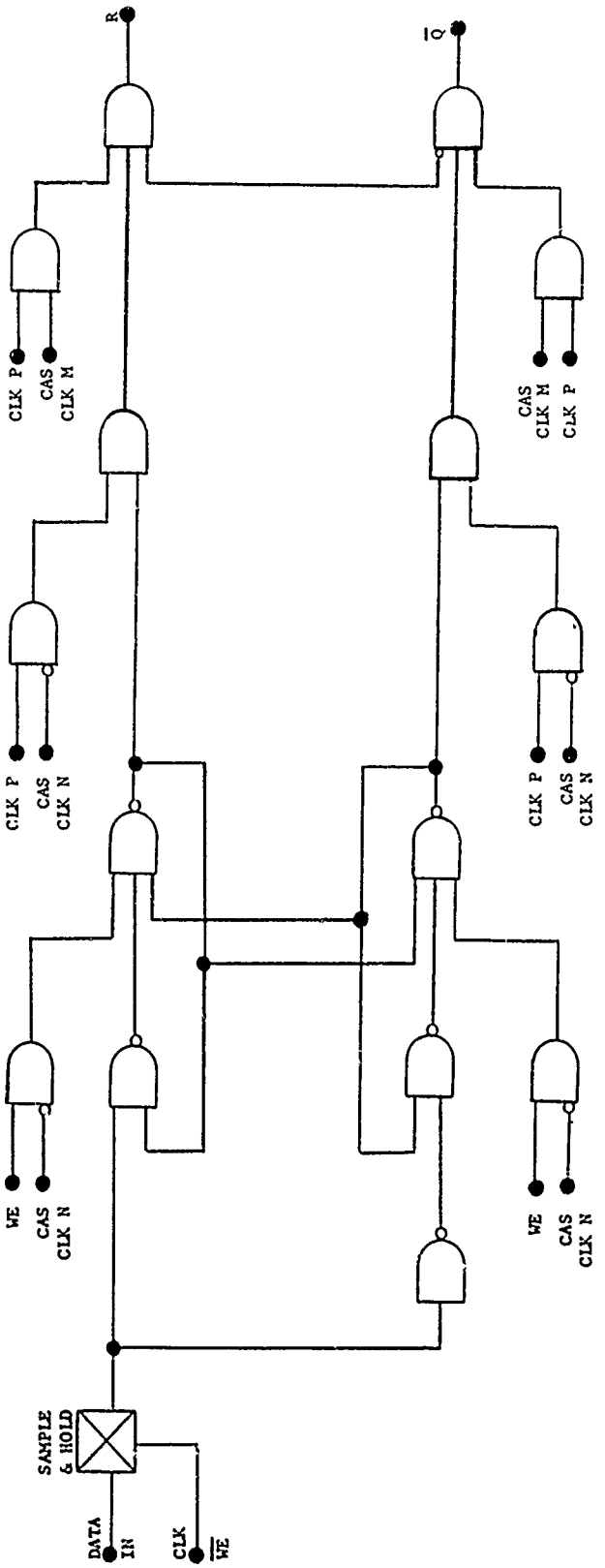


Figure 6-12 Logic Diagram, Data In Buffer/Latch

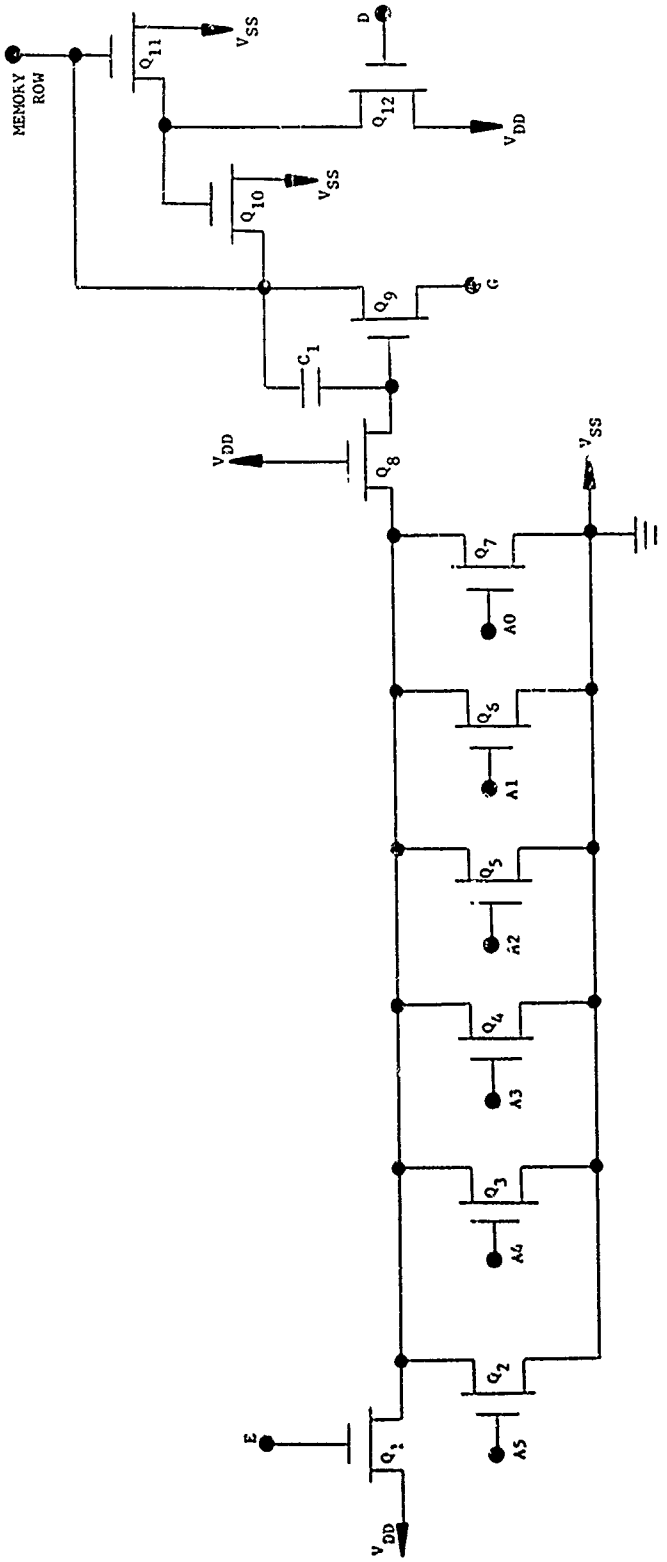


Figure 6-13 Schematic, Row Decode

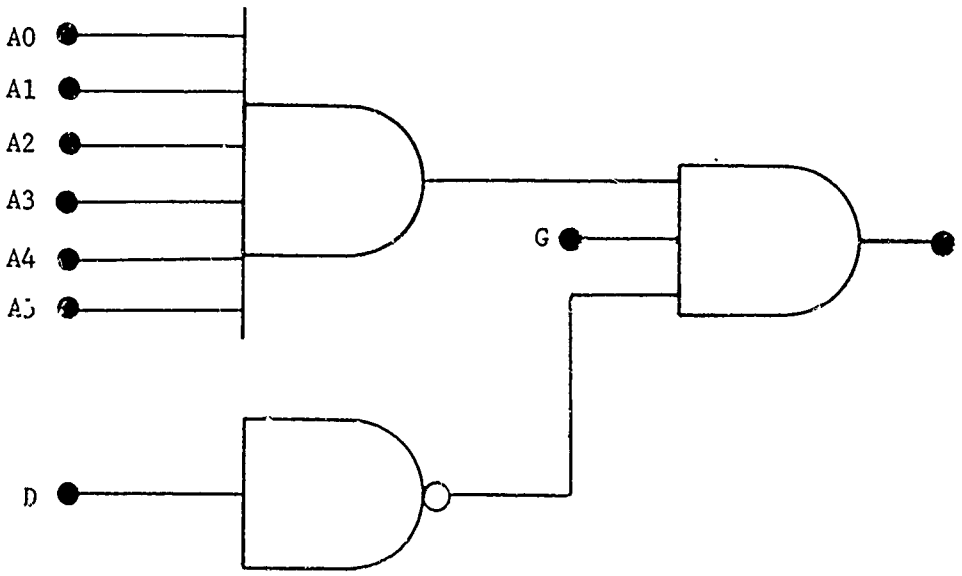


Figure 6-14 Logic Diagram, Row Decode (1 of 64)

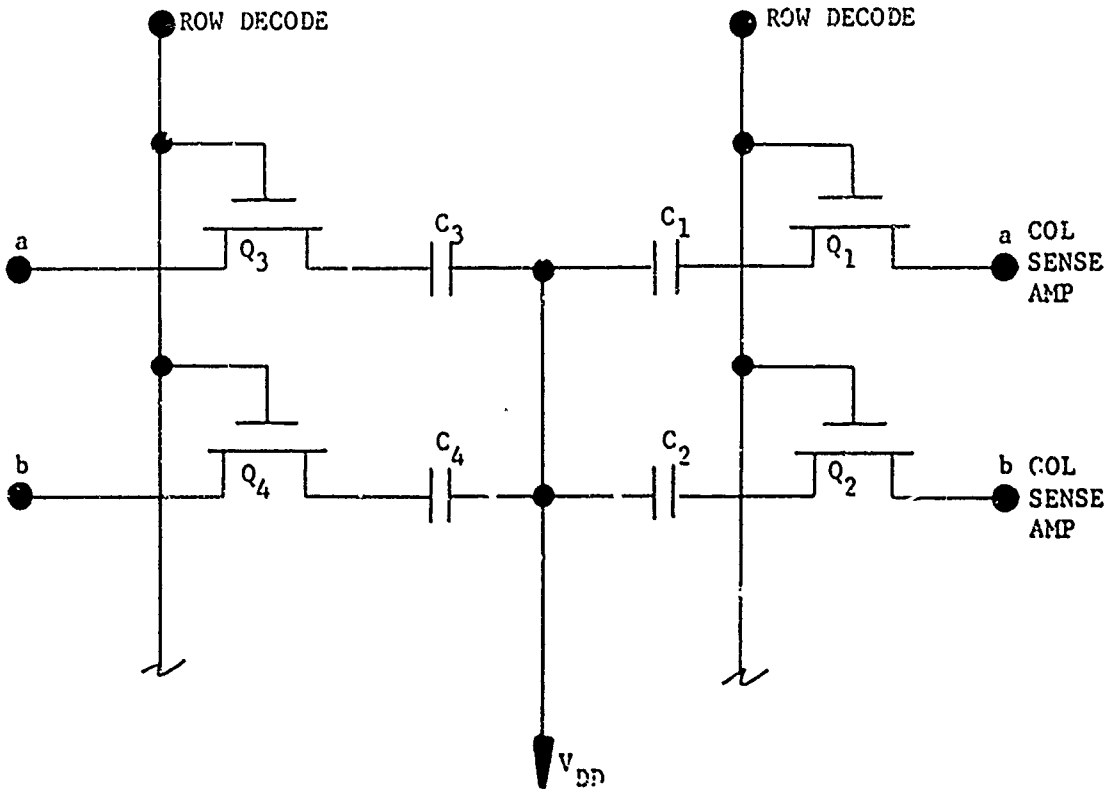


Figure 6-15 Schematic, Memory; 2 Cells

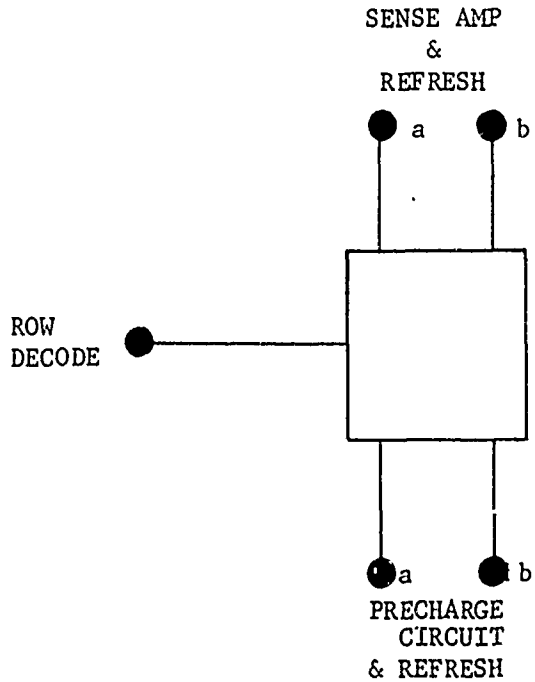


Figure 6-16 Logic Diagram, Memory Cell

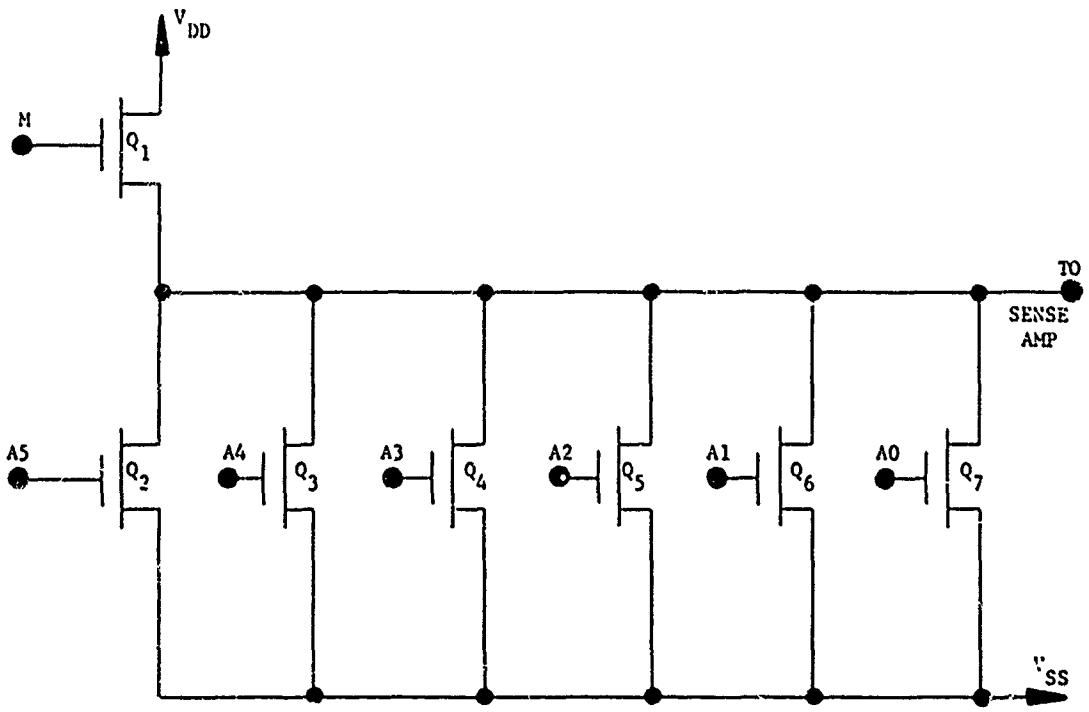


Figure 6-17 Schematic, Columnn Decode

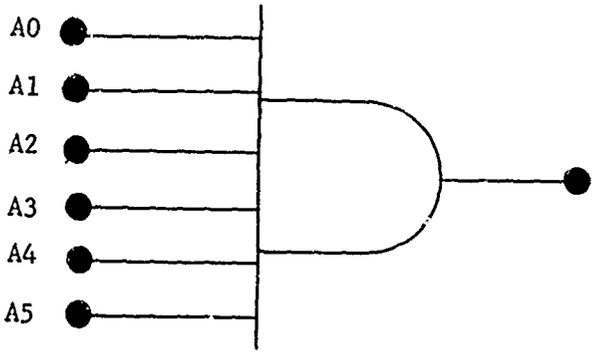


Figure 6-18 Logic Diagram, Column Decode (1 of 64)

$\overline{WE}$	COL DEC	O	$\overline{O}$	H	E	STATE
H	H	L	H	H	H	Precharge
H	L	H	L	L	L	Disable Refresh
H	H	H	L	L	L	Read
L	H	H	L	L	L	Write

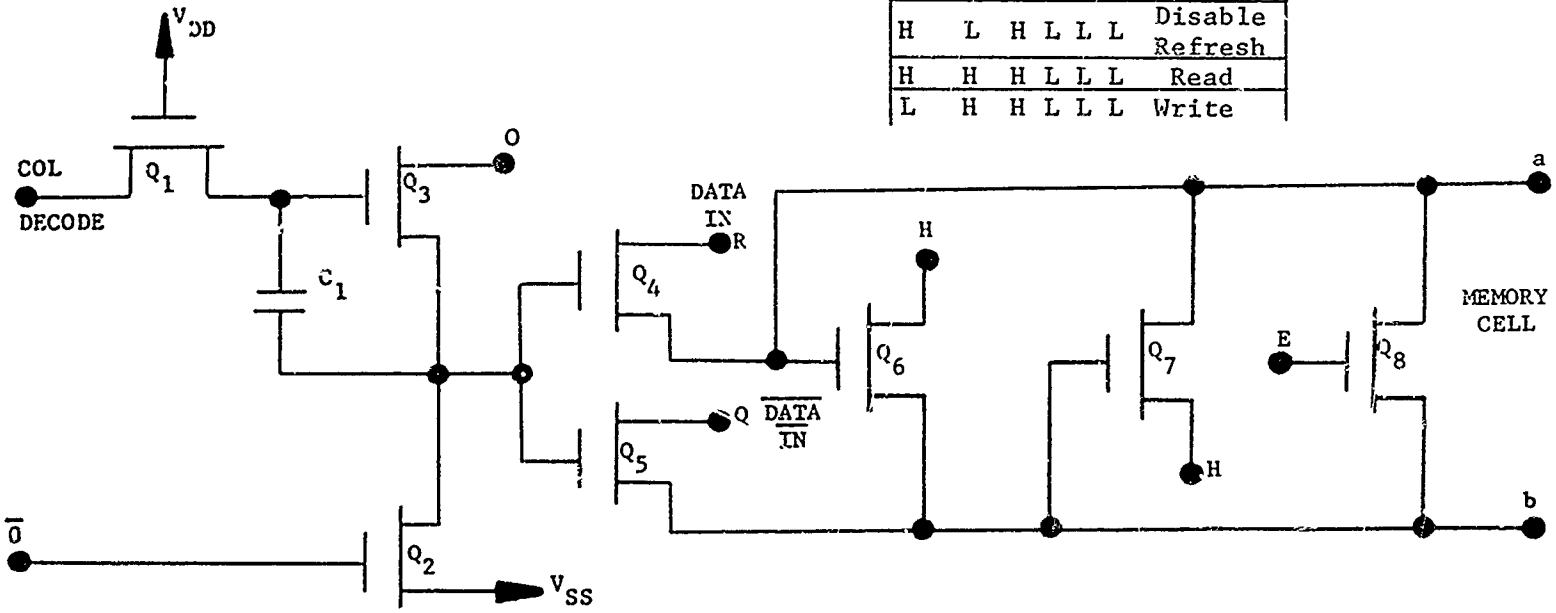


Figure 6-19 Schematic, Column Sense Amplifier

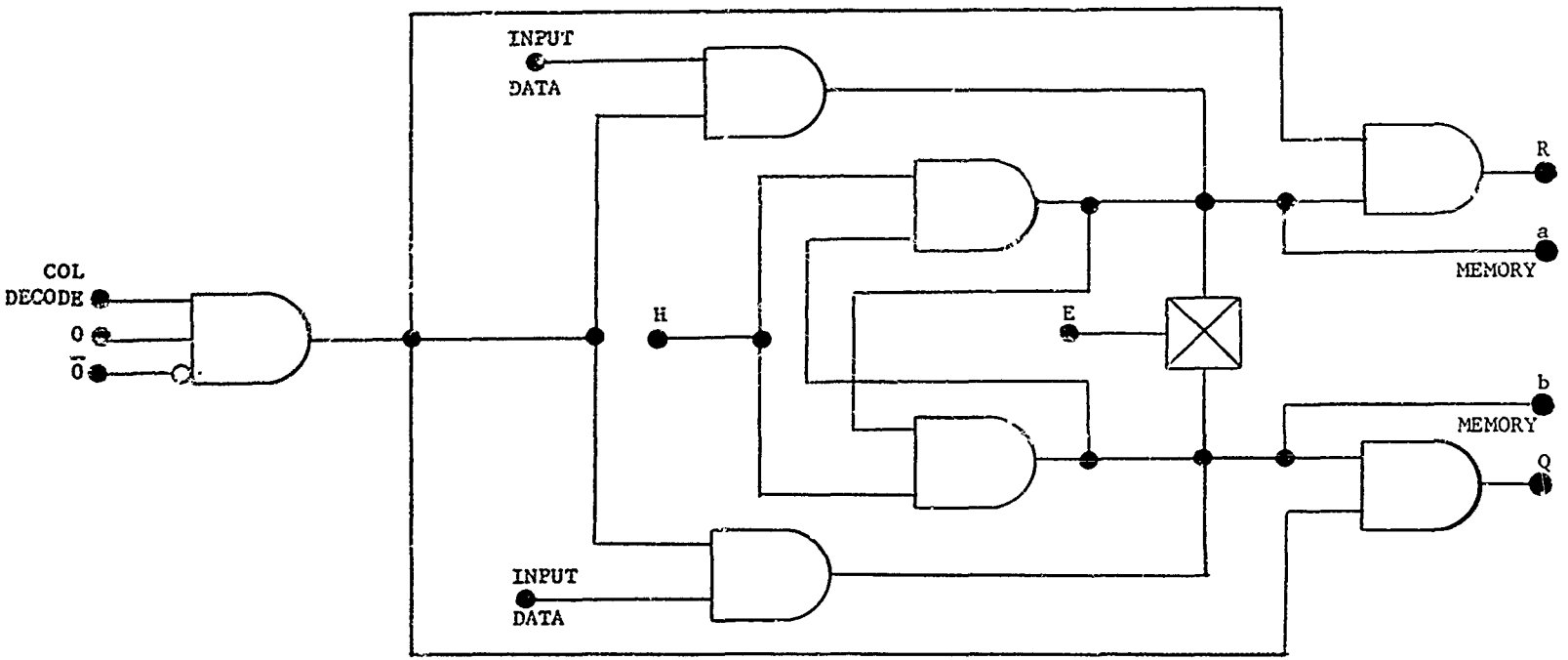


Figure 6-20 Logic Diagram, Column Sense Amplifier

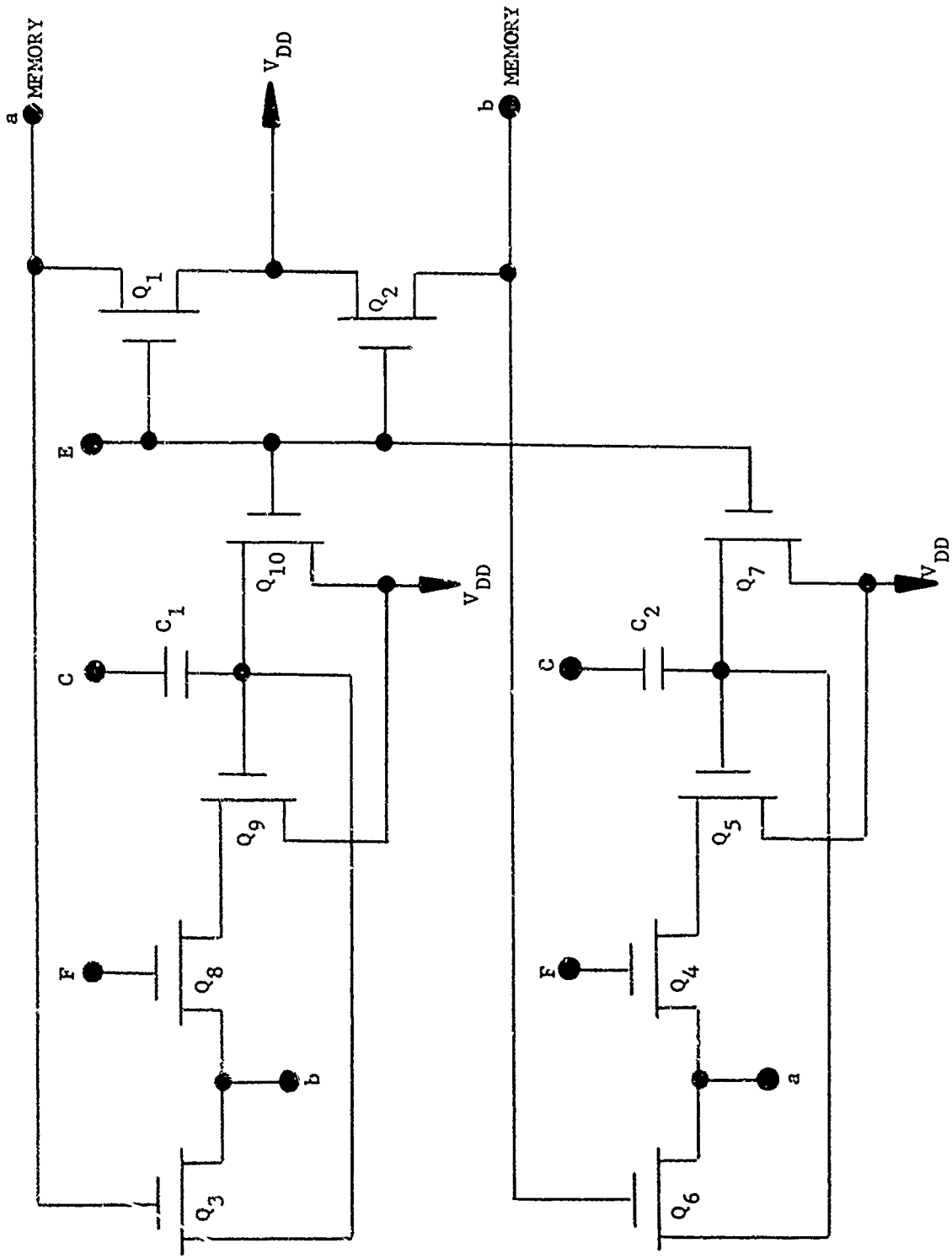


Figure 6-21 Schematic, Column Precharge/Refresh

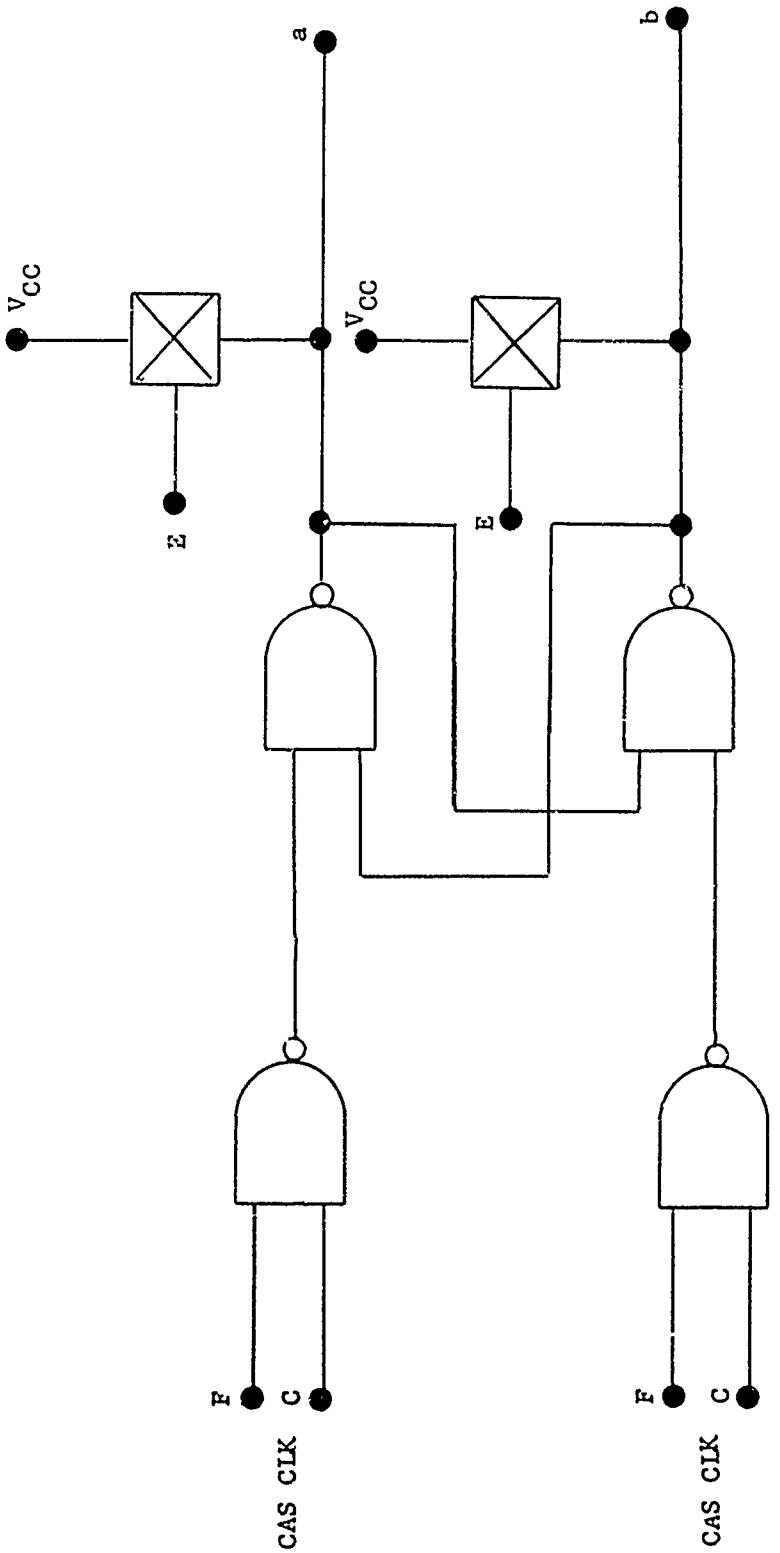


Figure 6-22 Logic Diagram, Column Precharge/Refresh

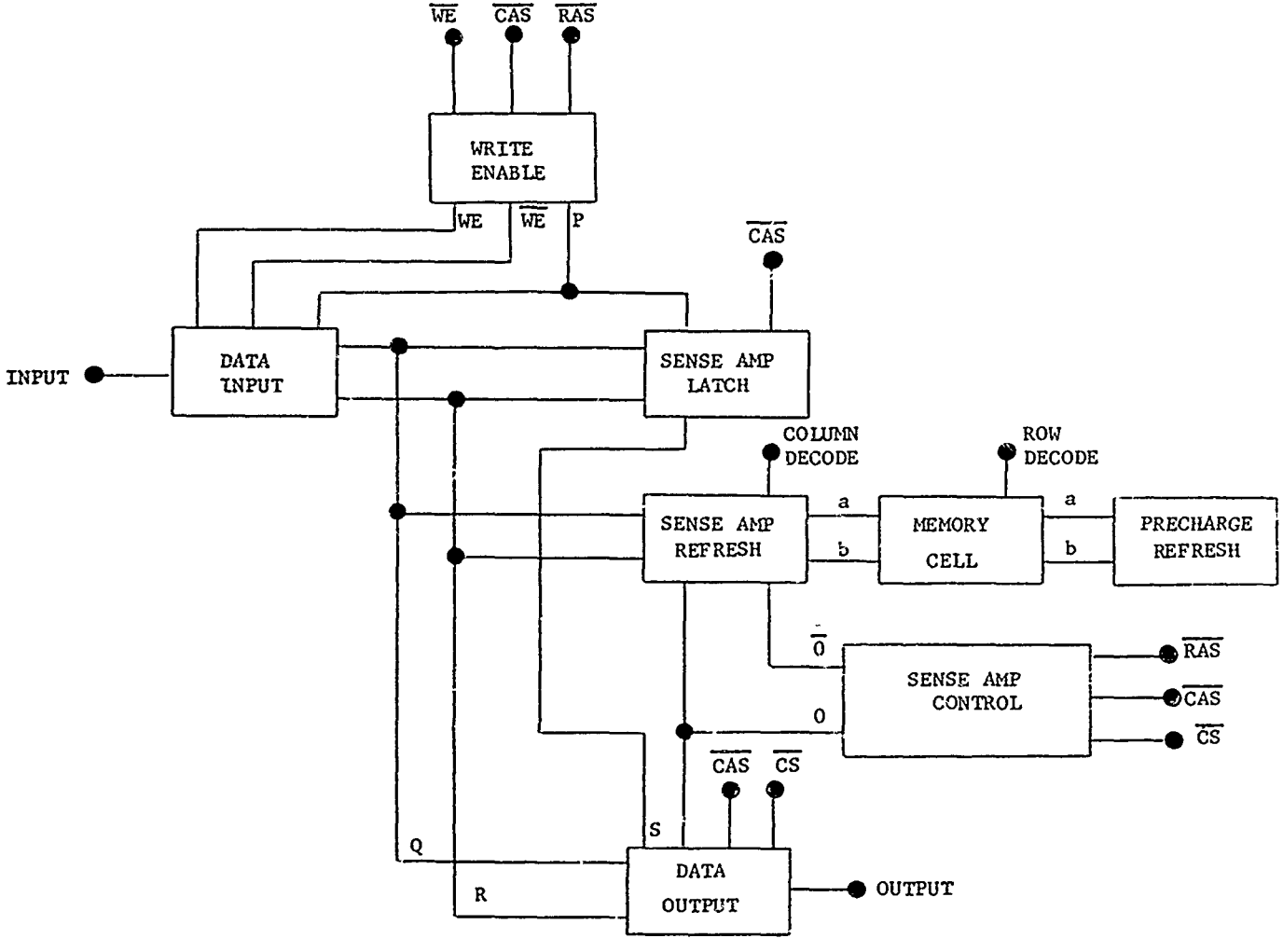
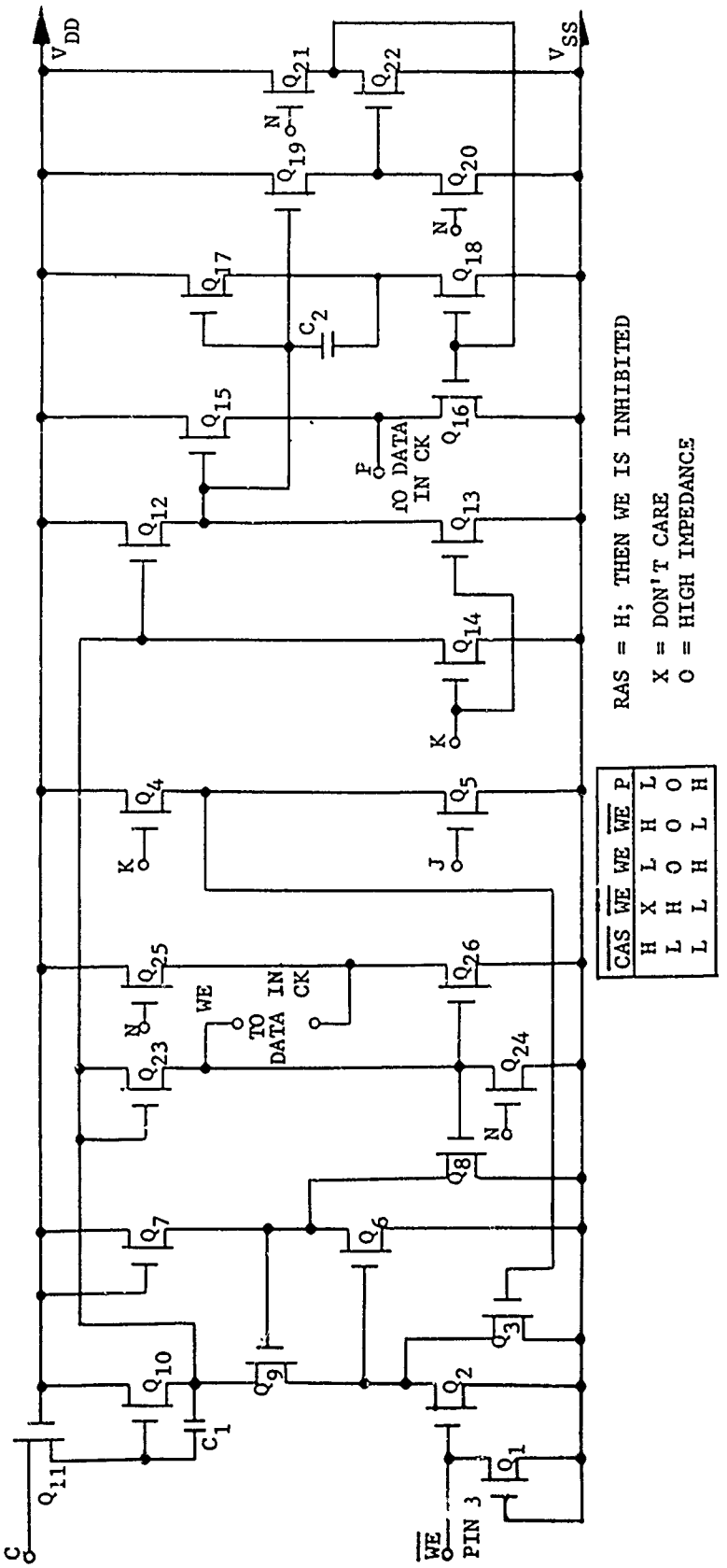


Figure 6-23 Block Diagram, Q/R Data Buss Interface



CAS	$\overline{WE}$	WE	$\overline{WE}$	P
H	X	L	H	L
L	H	O	O	O
L	L	H	L	H

RAS = H; THEN WE IS INHIBITED

X = DON'T CARE

O = HIGH IMPEDANCE

Figure 6-24 Schematic, Write/Enable

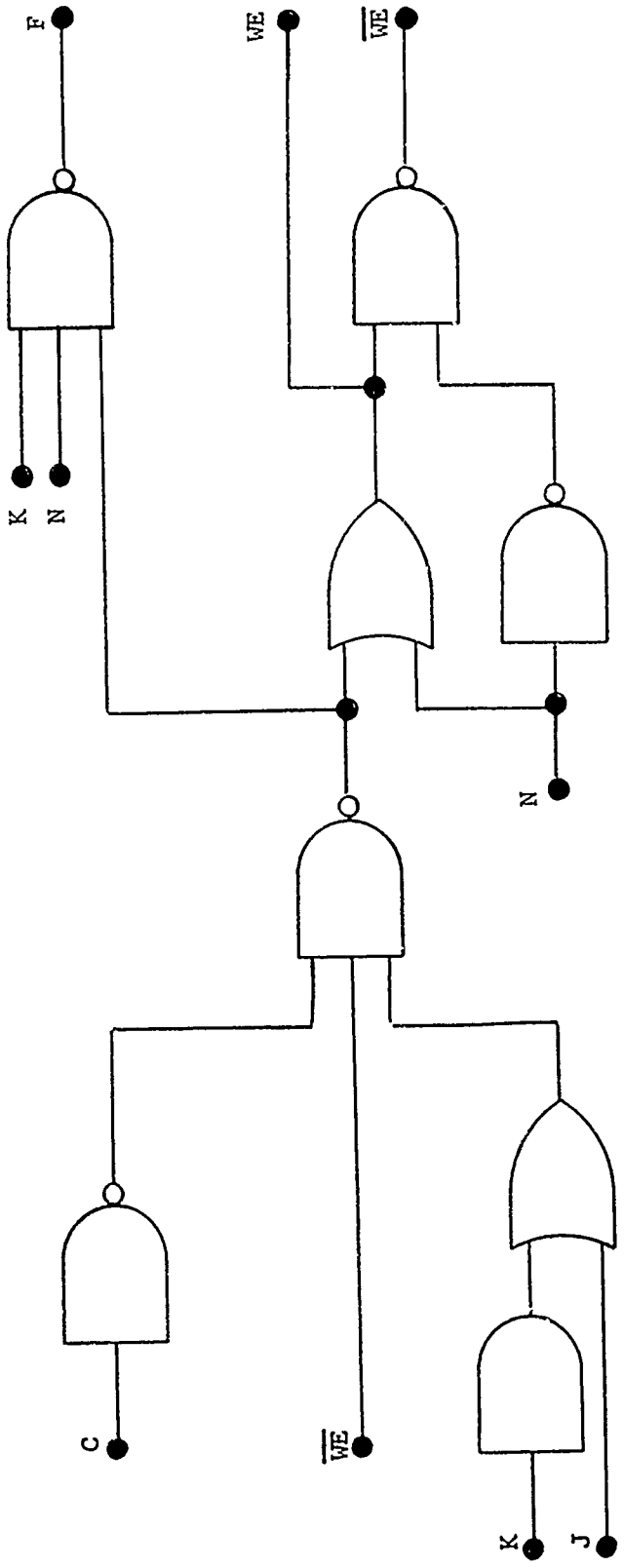


Figure 6-25 Logic Diagram, Write/Enable

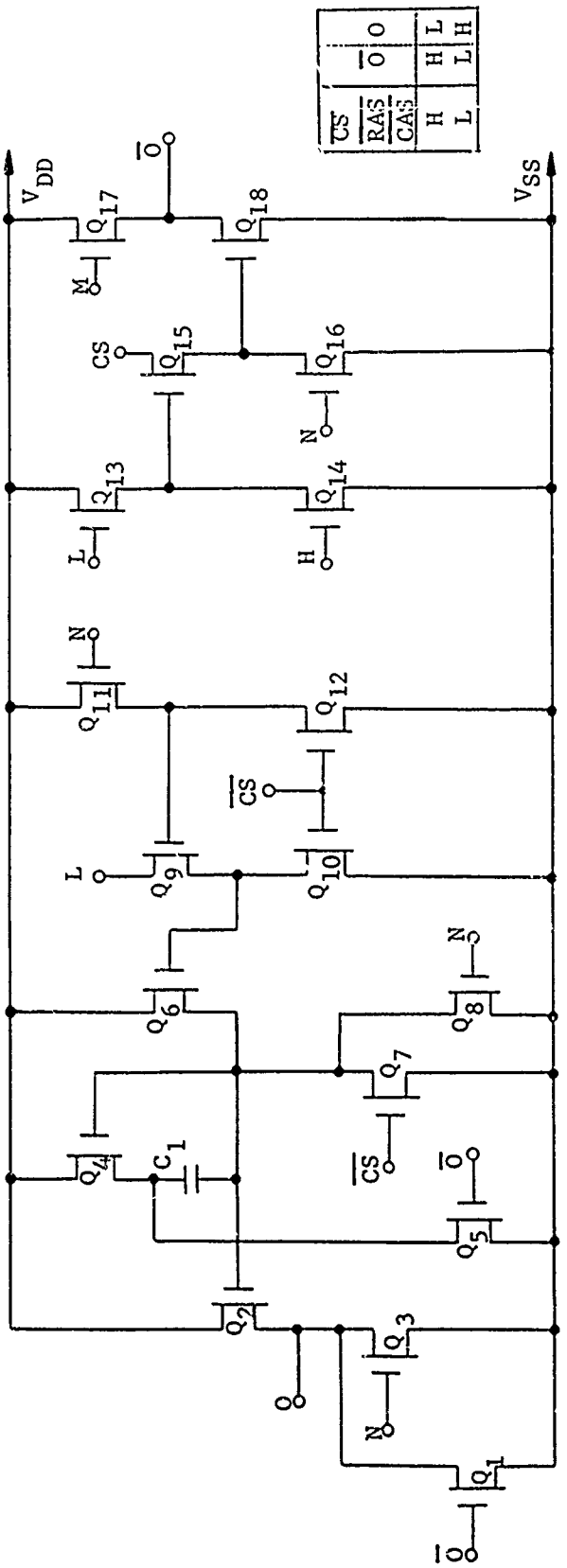


Figure 6-26 Schematic, Sense Amplifier Control

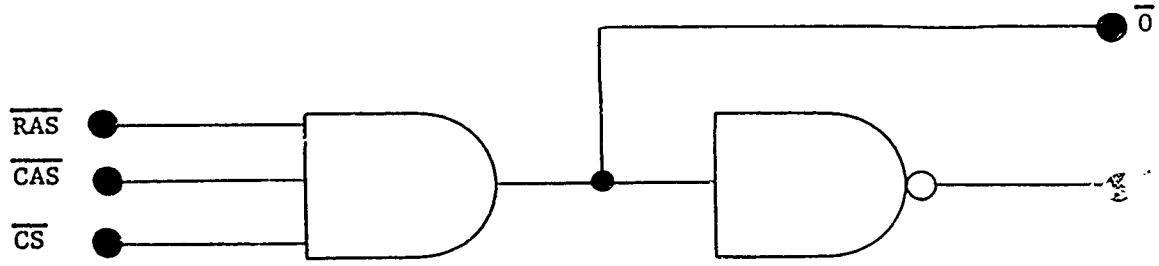


Figure 6-27 Logic Diagram, Sense Amplifier Control

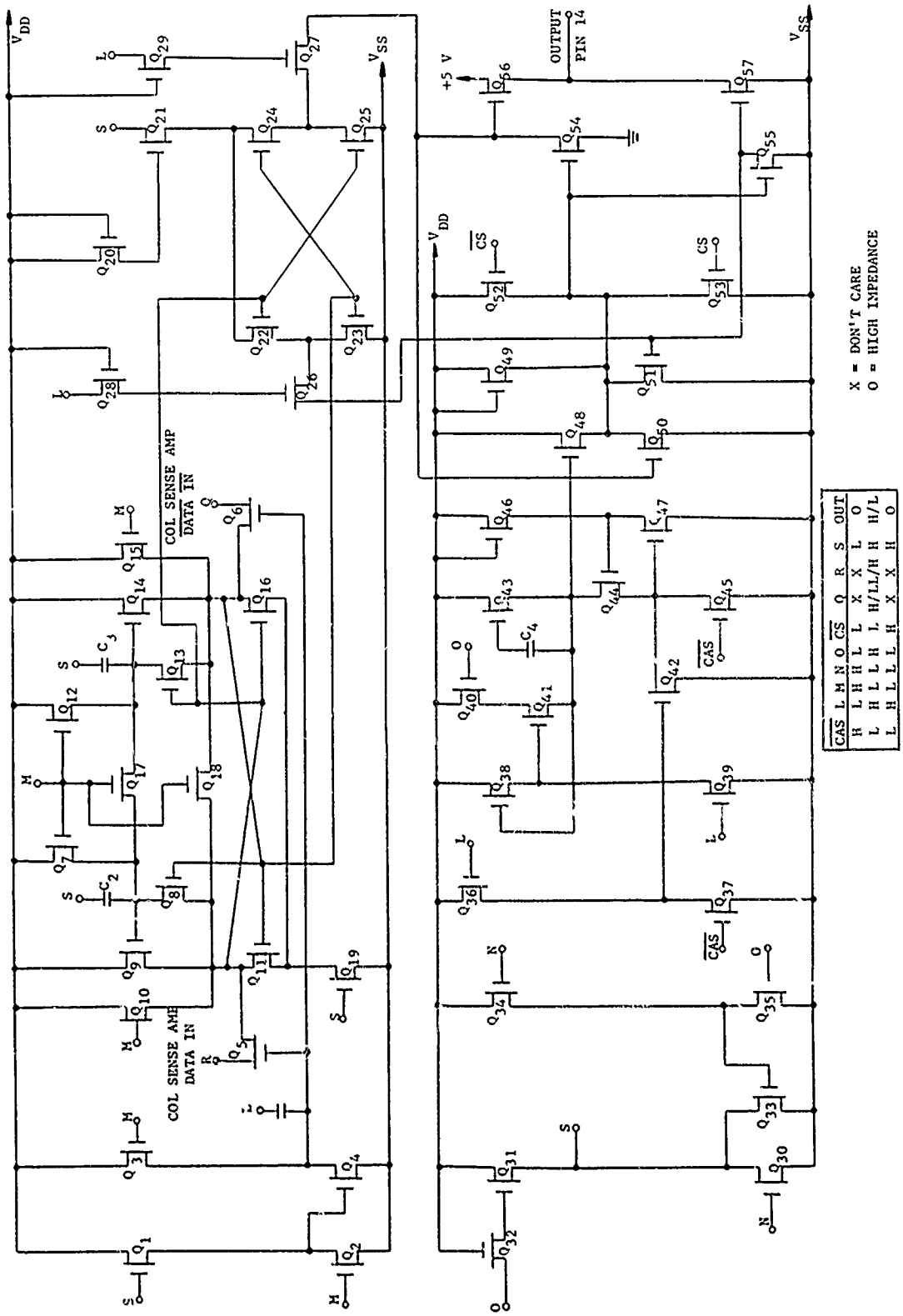


Figure 6-28 Schematic, Data Output

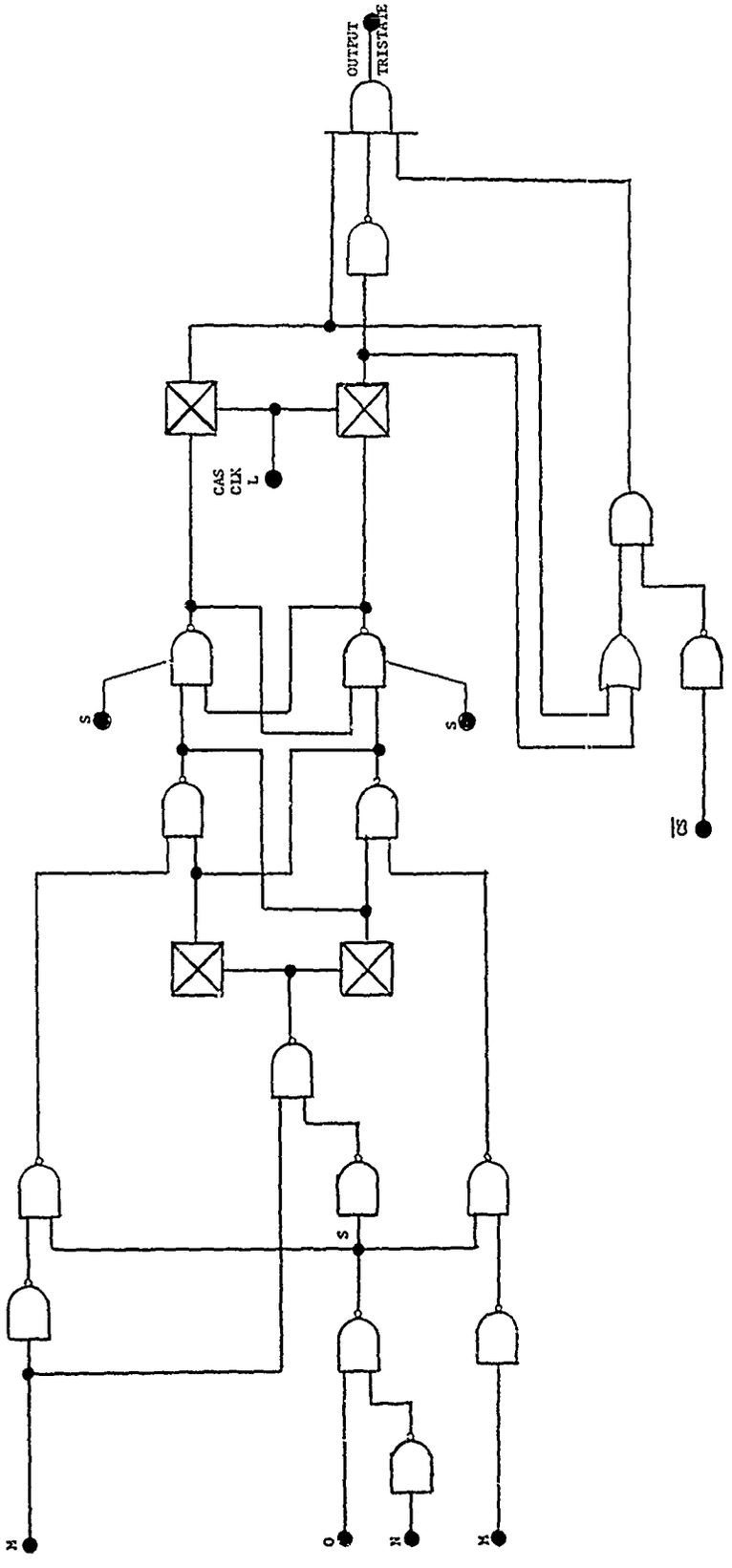


Figure 6-29 Logic Diagram, Data Output

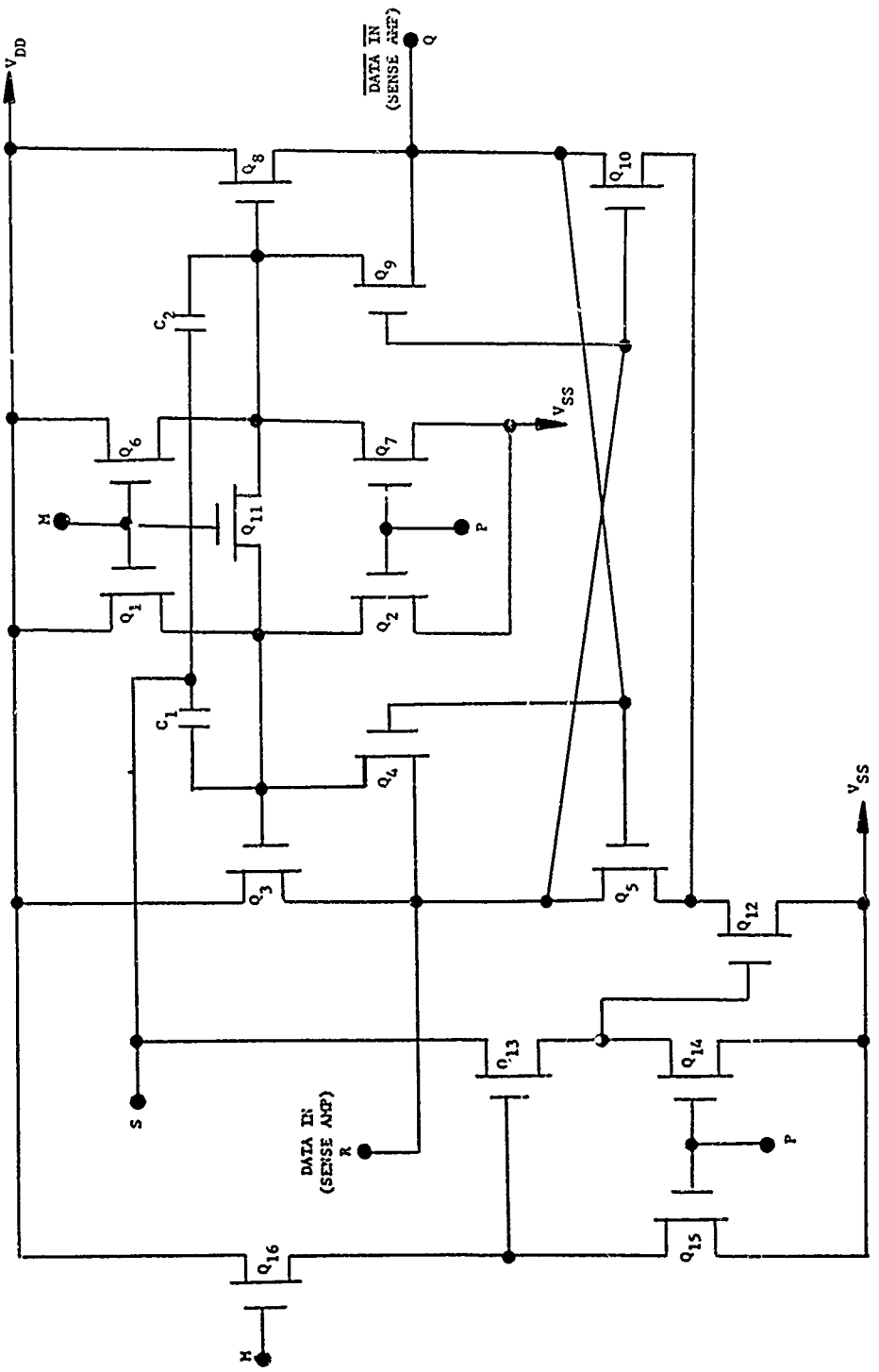


Figure 6-30 Schematic, Sense Amplifier Latch

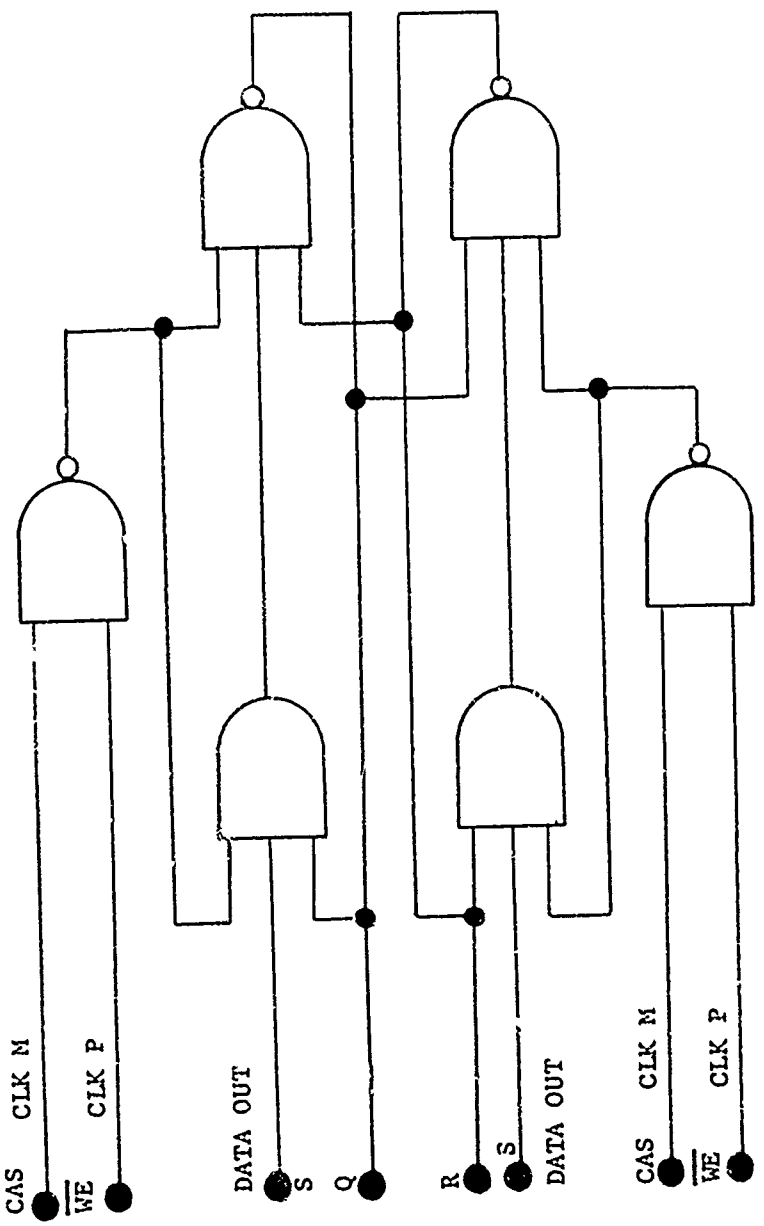


Figure 6-31 Logic Diagram, Sense Amplifier Latch

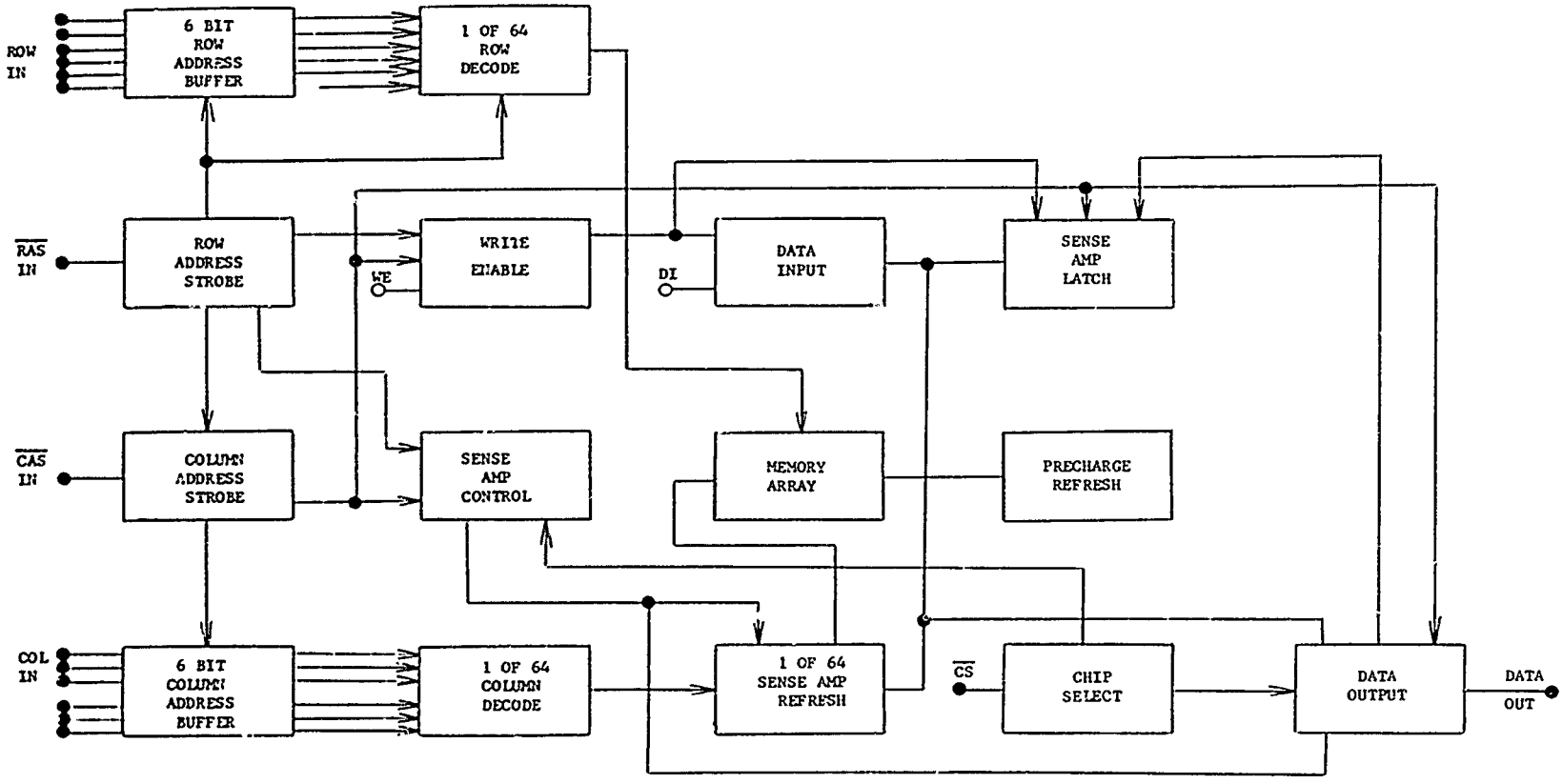


Figure 6-32 Block Diagram

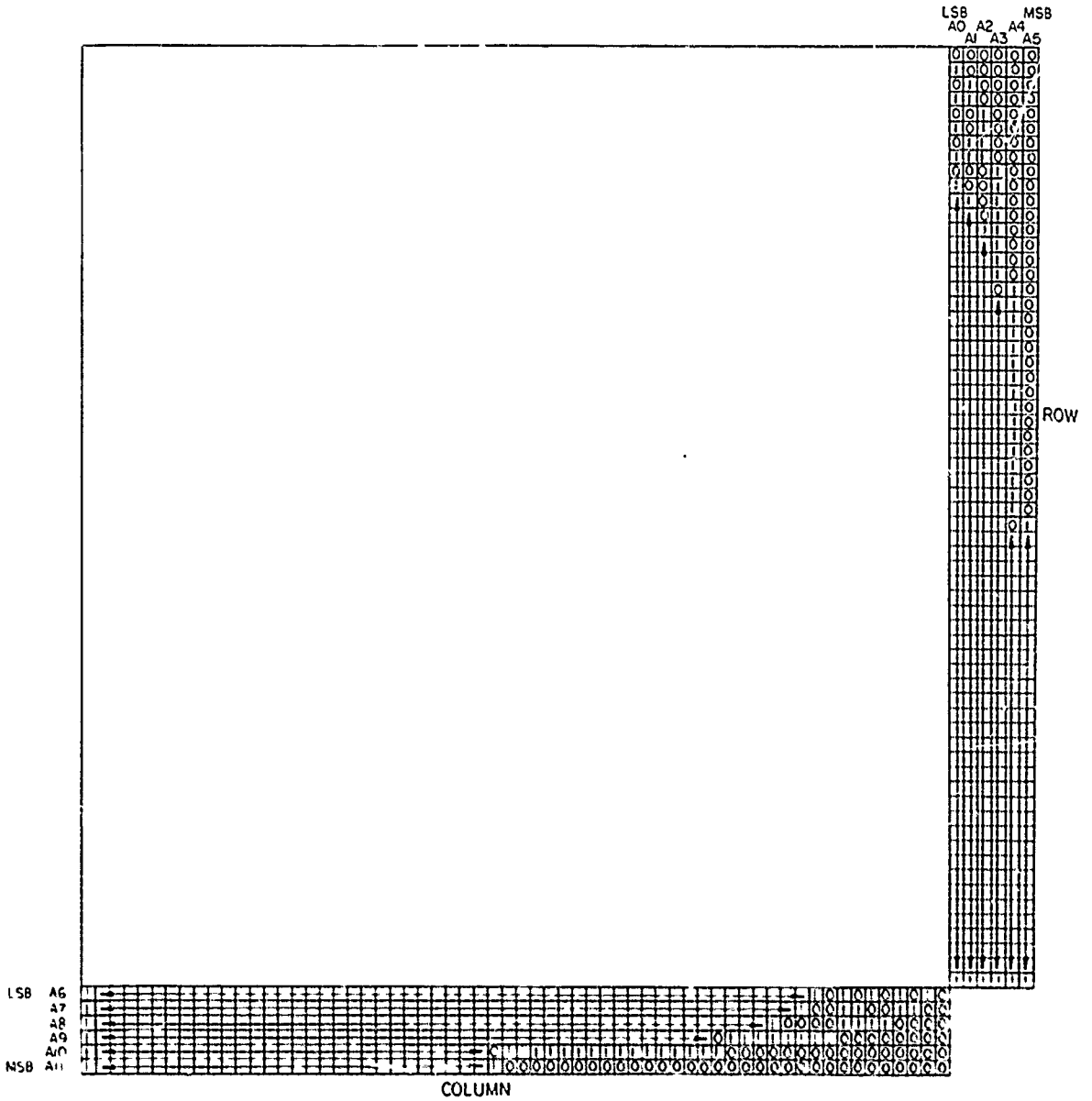


Figure 6-33 Bit Map

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4.7 4096 BIT DYNAMIC RAM (I^2L BIPOLAR)

Device Description

This device is a bipolar Isoplanar I^2L dynamic 4096 x 1 bit RAM circuit. This circuit utilizes a single 5 volt supply voltage. It is packaged in a 16 lead ceramic dip with a KOVAR lid. The device contains two chip select inputs and a three state output.

Electrical Characterization

At the time of this evaluation this device type was not available from the supplier. Twelve devices were supplied for this study by RADC. Two devices were identified as failures and ten were functionally good devices.

The ten good devices were electrically tested in accordance with the suppliers data sheet. These devices were serialized as received and the identified serial numbers were maintained. The DC parameters were measured, recorded and are listed according to serial number in Table 7-I. All parameters were verified to meet the manufacturer's specifications. The IIH parameter for S/N 34, pin 15 exhibited a gradual increase in leakage current with voltage applied.

The functional testing of this device presented some different timing requirements. This device also employs multiplexed row and column address lines. However for this device, only the row address states are strobed and there are 5 row address inputs and 7 column address inputs. This required an unbalanced address multiplexing scheme. Memory refreshing is accomplished by row addressing and the maximum specified refresh interval is 2 ms. The row addresses are strobed and latched on the positive transition of the address enable signal. The signal timing constraints were not as severe for this device as for the NMOS dynamic RAM. It was necessary to decouple the 5 volt supply line at the test socket to obtain consistent device performance.

The ten devices were tested functionally. Of these ten devices, five were shown to be totally functional, four partially functional; and one, S/N 34, nonfunctional. The four partially functional devices exhibited intermittent data errors which were common to specific addresses. The cause was suspected to be improper signal timing margins. A recheck of the applied address signal timing did not identify a timing problem. This problem was not pursued further as five functional devices would be sufficient for this task. The functional test frequency (LSB) was 40 kHz. Photo 7-1 shows typical address signals supplied to this device by the functional test circuit. As described previously, the timing format is divided into four periods; buffer, refresh, buffer, read/write, and back to buffer. The refresh and read/write segments are identified in Photo 7-1. As mentioned previously the five row address signals are multiplexed on this device. The row address states are latched into the row address latch/decoder circuits on the positive edge transition of the address enable (AE) signal. The row address inputs must remain stable for a minimum of 35 ns after the positive AE transition. After this period the column address states are applied and the

circuit operates like a static RAM. 75 ns after column address the output data is valid and remains valid for approximately 10 ns after AE goes high, chip select (CS) goes low or the column address inputs change. Additional memory words can be accessed from the same row initially addressed by changing the column address. Following the column address access time of 75 ns, the data at the output will be valid for the second column addressed memory location. In the example shown in Photo 7-1, the circuit is write enabled and is writing a high data state. The AE refresh clock rate is 125 kHz and the AO row address refresh clock rate is 63 kHz.

Package Delid and Glass Passivation Removal

The package was opened by grinding the metal lid using 400 grit abrasive paper. The grinding is stopped, when the lid is thinned to a point where it "oil cans" and prior to breaking into the package cavity. The lid is then carefully penetrated with a sharp probe and the lid is peeled off the package.

Removal of the glass passivation was evaluated using the partially functional devices. This device utilizes a single level aluminum metallization and as a bipolar device should easily tolerate glass passivation removal. Initial light microscope examination of the die surface showed a black appearance with limited ability to distingish metal conductors. This is indicative of a sputtered quartz passivation. It has a rough surface which scatters the light and is hard to illuminate. The black appearance made it difficult to estimate the passivation thickness. The etchant used for passivation removal was the glycerine stopped buffered HF etch. The etch used was:

125 ml hydrofluoric acid	48%
25 ml nitric acid	70%
250 ml glycerine	

A number of problems were encountered in removing the passivation. The first problem was determining the point where sufficient glass had been removed. Once the sputtered glass was removed there was no thermal oxide color visible. Glass etching was continued without seeing any indication of oxide color. This resulted in functional failure of the device. The integrated injection logic technology was expected to exhibit an unfamilar surface appearance. This by itself would not have presented too much of a problem, but it became apparent there were other differences. Further examination showed that the Isoplanar processing further complicated visual evaluation of the passivation etching progress. In the Isoplanar process, vertical cell isolation is accomplished by dielectric or SiO_2 isolation. This dielectric is very thick as compared to the surface thermal oxide covering the diffusion cells. Therefore, this thin oxide can be easily removed and if etching continues the isolation oxide can be removed to an extent that cell junctions are exposed. The circuit will not remain functional when the surface oxide integrity is compromised. It was decided that the die surface should be etched to the point where the majority of the sputtered glass had been removed. This would keep the surface oxide intact.

The glass removal evaluation showed the typical etch time to remove the sputtered glass was 30 seconds. After 30 seconds it appeared that considerable glass remained. Following etching the device was cleaned in detergent and ultrasonic for about 2 seconds (dipped in and out) and rinsed with DI water, isopropyl alcohol, and gently dried with dry nitrogen. This wash was very effective in removing glass residue without overexposure to etching. If the passivation was removed totally by etching, (without additional cleaning) it was found the circuit would not remain functional.

S/N 41 was etched for 30 seconds and cleaned. The circuit remained functional. Light microscope examination showed speckled residue of passivation remained. The device was determined to be acceptable for SEM evaluation. Photo 7-2 is a photograph showing the overall die.

Circuit Characterization

Device S/N 41 was placed in the SEM for initial voltage contrast evaluation. The acceleration voltage used for examination of this device was 1.2 KV. This voltage was used to reduce the effects of surface charging on voltage contrast. The typical variations of circuit node voltages in I^2L circuits are 0.3 to 0.7 volts. These variations represent a true challenge for photographic portrayal using a nonlinear secondary electron detection system. Initial voltage contrast examination of this circuit showed very limited candy stripe contrast.

Before circuit characterization could be started, the basic cell structure and circuit scheme must be known and identifiable. The die was examined by SEM and light microscopy to establish a method for cell identification and circuit interconnections. In typical I^2L circuitry, a basic cell consists of a lateral PNP transistor which acts as a current source and an NPN vertical or PLANAR transistor which acts as a switch. The PNP is referred to as an injector. The NPN is usually operated in the inverted mode and the emitter connection is made through a buried layer. This technology does not usually utilize diffused resistors. Examination of the circuit and attempts to identify basic cell structures were mostly unsuccessful. No correlation could be made to locate either the PNP or NPN structure.

The circuit was examined using EBIC and a very important application was identifed. Using EBIC it was easy to locate major diffusion cells and most important locate buried layer interconnections. The value of this application will be more fully appreciated later in this report. Two key questions remain to be answered. What is the type of basic cell structure utilized, and how can the surface connections to a cell be distinguished from one another; i.e., which connect to N diffusions and which connect to P diffusions?

A literature search was made to locate information directly related to Isoplanar I^2L RAM circuits. This search located a minimum of related literature. For the most part it described the memory cell structure.

One of the circuits was mechanically probed to measure node voltages for different conduction states. These data were inconclusive because of low

level node voltage changes. It was still not certain what signal was related to the cell input or output. This is compounded by the inaccessible connections located subsurface.

The circuit was mechanically probed using a curve tracer to identify junction polarities. With these data it seemed the cell structure could be developed. In retrospect, the key problem was attempting to correlate these data with the typical PNP injector/NPN switch transistor I^2L circuit cell.

Contact was made with the manufacturer through the local field representative. The data collected to this point and the basic questions that we had not answered were discussed by telecon with a product design engineer responsible for this part. He was advised of our intentions and asked that any information provided be nonproprietary. Our basic questions were answered and copies of published articles related to this technology were provided. The three key factors which were provided are; this device is constructed using a P epitaxial layer on a P substrate, the peripheral circuits employ primarily NPN planar transistors, and the collector contacts are made subsurface to buried layers. The N doped buried layers are located beneath the epitaxial layer.

At this point one problem remains. It is distinguishing emitter contacts from base contacts. It was thought this could be done using EBIC. The emitter diffusion cannot be identified by EBIC because it is extremely shallow. It is suspected that this junction is ion implanted. Because it is very shallow, it provides a very narrow capture cross section for beam induced carriers. It still could be possible using different electron beam parameters, but time was not available for evaluation.

A review of the mechanical probe/curve tracer data and light microscope examination of the circuit produced a method of base/emitter identification. A narrow band of thermal oxide (typically 4 to 6 microns wide) was identified immediately adjacent to the connecting metal stripe. These oxide bands were common to the respective diffusions and exhibited different colors; i.e., for this device the oxide common to N diffusions were blue and P diffusions were green. The oxide bands were found to be present for all diffusions.

Because of the time expended to identify a procedure for developing a circuit schematic for Isoplanar I^2L, there was only sufficient time remaining to apply this procedure to one functional circuit. The A0/A1 row and column address/encode circuit was selected for definition.

The secondary electron image (SEI) of this circuit is shown in Photo 7-3. Note the "1" and "U" shaped elements located in the right center of Photo 7-3. These elements do not appear to be connected in the circuit. Photo 7-4 is the EBIC image of this same circuit. This photo was taken with pins 1, 2, and 16 connected to the SCA and pin 8 connected to ground. The beam voltage was 15 KV. Note the black buried layer interconnects and specifically those connected to the ends of the "1" and "U" shaped elements. These subsurface interconnections have dramatically reduced the metal interconnect density on the surface. The outputs from this row and column address/encode

circuit, are the four buried layer conductors, leaving the center of Photo 7-4 and traveling toward the top. The two on the right are partially obscured by the V_{CC} buss metallization. The voltage contrast micrograph for this circuit is shown in Photo 7-5. This photo was taken with A0 cycling at 1.2 Hz between 1 volt and 2 volts, A1 and AE were high, and CS was low. Swinging A0 between 1 and 2 volts rather than 0 and 5 volts was very effective in reducing bleed over from the interconnect wire. Swinging the input signal between 1 and 2 volts crossed the input threshold and represented a logical 0 and 1 level. The contrast was enhanced in Photo 7-5 to increase the sensitivity to circuit node voltage changes. Photo 7-6 is the light photograph of this circuit. The black speckle in this photo is the sputtered quartz passivation residue. The first appearance of this circuit in the light photograph tends to oversimplify its complexity.

These photographic data were used to develop the circuit schematic. The key data were the EBIC and light photographs. A light photo was identified by colored ink to locate the P and N diffusions. Identification was performed with the light microscope and the photograph was marked accordingly. The voltage contrast micrograph also provided useful information. The relative voltage levels and input signal response were used in verifying the circuit schematic. The schematic is shown in Figure 7-1. This circuit represents two row and column address buffers and the encoders for these addresses. A clock from the address enable circuit, identified as AE-NOT, controls these circuits by enabling the circuit ground references. This enable circuit consists of Q19, 29, 21, and associated circuitry. This circuit provides an enable during row and column addressing. The A1 and A0 addresses set the states of Q3/Q4 and Q8/Q9. These states are encoded by diodes D8 through D15. The encoded addresses are applied to buffers Q11 through Q14 and Q15 through Q18. The Truth Table for address encoding is included in Figure 7-1. The buffer outputs are then applied to the row and column tree decode circuits. These output interconnects are made through buried layer conductors to metal conductors located on the other side of the V_{CC} buss. The row address latch circuit is apparently located in the row tree decode circuit. The Logic Diagram for the row and column address buffer/encoder circuit is shown in Figure 7-2.

There was not sufficient time remaining to characterize the remainder of this circuit or evaluate the feasibility of failure isolation. Had there been available time, it is believed that these items could have been completed successfully. The procedures developed are applicable to the remaining circuits. The complete die was examined using EBIC and the response obtained was very good. Photo 7-7 is the SEI photograph of the complete die. Photo 7-8 is the EBIC micrograph taken at the same magnification as Photo 7-7. This photo was taken with pin 16 connected to the SCA and pin 8 connected to ground using a beam voltage of 15 KV. The EBIC photo shows good response from all areas of the die. Numerous buried layer interconnections are vividly displayed. Some of the more obvious are interconnects with address/encoder circuit outputs and interconnects with row and column tree decode inputs. These interconnections appear as dark stripes in the EBIC photo. These buried layer interconnections are essentially undetectable by any other means. Portions of these buried layers could be seen using low magni-

fication light microscopy, but this was not adequate for locating and identifying the points of interconnections.

The characterization of this circuit provided the most demanding test of available evaluation techniques and applications. Even though they stood up well to the test it is felt that additional improvements are needed and can be developed. Two important areas would be increasing the voltage contrast detection sensitivity and developing the EBIC methods for identifying the N and P diffusions in individual transistor cells.

The I^2L technology presents some difficult obstacles to present day failure isolation techniques. It appears that electron beam techniques must be employed, and further development of these techniques are needed to improve their application and hopefully reduce their risk. Even without these developments the electron beam techniques are superior to any other practical techniques which are currently available.

TABLE 7-I DC PARAMETERS

Date Code 7715

SN31	SN32	SN33	SN34	SN41	SN51	SN52	SN54	SN61	SN62	
.29V	.30	.30	.29	.29	.29	.28	.26	.31	.28	V_{CC} = 4.75V
										I_{OL} = 15 mA
										V_{OL} Max = 0.5V
2.61V	2.66	2.62	2.59	2.68	2.63	2.64	2.66	2.61	2.70	V_{CC} = 4.75V
										V_{OH} I_{OL} = 5mA
										V_{OH} Min = 2.4V
-.87V	-.88	-.82	-.82	-.86	-.86	-.86	-.72	-.87	-.86	A0 Pin 1
-.98	-.97	-.91	-.91	-.94	-.92	-.92	-.81	-.95	-.94	A1 Pin 2
-.71	-.77	-.72	-.69	-.74	-.77	-.76	-.56	-.77	-.69	A2 Pin 3
-.68	-.74	-.70	-.66	-.72	-.74	-.74	-.54	-.73	-.65	A3 Pin 4
-.61	-.69	-.63	-.61	-.67	-.63	-.63	-.48	-.65	-.61	A4 13
-.64	-.70	-.65	-.62	-.67	-.63	-.64	-.49	-.66	-.62	A5 14 V_{CD}
-.58	-.66	-.60	-.66	-.62	-.57	-.59	-.41	-.61	-.58	A6 15 V_{CC}=5.25V
-.92	-.93	-.92	-.90	-.91	-.90	-.90	-.82	-.91	-.89	AE 12 I_{in}= -10mA
-.75	-.80	-.85	-.72	-.77	-.79	-.79	-.6i	-.79	-.72	LE 6
-.89	-.90	-.84	-.86	-.86	-.84	-.84	-.77	- 85	-.87	D_{in} 10
-.70	-.74	-.72	-.67	-.72	-.74	-.73	-.55	-.73	-.67	CS_1 5
-.84	-.88	-.85	-.83	-.83	-.84	-.84	-.76	-.86	-.87	CS_2 9
-.75	-.77	-.77	-.74	-.77	-.74	-.63	-.63	-.75	-.75	WE 11
										V_{CD} Max = 1.5V

TABLE 7-I (cont.)

Date Code 7715

SN31	SN32	SN33	SN34	SN41	SN51	SN52	SN54	SN61	SN62	V_{CC} = 5.25V Pin Number	Meas.
-42uA	-50	-49	-46	-57	-50	-50	-44	-19	-46	1	I_{IL}
-44	-44	-52	-47	-55	-54	-52	-44	-19	-50	2	
-40	-48	-47	-45	-56	-49	-49	-42	-18	-43	3	
-38	-43	-45	-39	-51	-46	-47	-38	-17	-42	4	
-37	-43	-43	-38	-50	-41	-43	-37	-17	-39	5	
-42	-49	-49	-44	-57	-49	-51	-42	-20	-45	6	
-41	-45	-47	-41	-53	-45	-47	-40	-19	-45	9	
-42	-45	-48	-43	-54	-47	-48	-43	-19	-45	10	
-43	-48	-48	-43	-57	-49	-50	-42	-20	-46	11	
-61	-65	-67	-62	-79	-68	-69	-63	-28	-65	12	
-38	-44	-43	-40	-52	-45	-46	-39	-18	-41	13	
-42	-45	-46	-43	-54	-46	-46	-43	-18	-45	14	
-55	-61	-62	-56	-74	-63	-63	-55	-24	-59	15	
										I_{IL} Max = 400uA	

TABLE 7-I (cont.)

SN31	SN32	SN33	SN34	SN41	SN51	SN52	SN54	SN61	SN62	V_{CC} = 4.5V PIn Number	Meas.
1.2uA	1.51	1.2	1.3	.17	1.6	1	.8	1.4	1.2	1	I_{IH}
1.2	1.6	1.3	1.3	1.8	1.7	1.6	.9	1.4	1.3	2	
1.2	1.6	1.3	1.3	1.8	1.8	1.6	.9	1.5	1.4	3	
1.3	1.7	1.4	1.4	2.0	2.0	1.8	1.0	1.6	1.5	4	
3.9	3.4	3.8	3.8	2.6	3.7	3.7	3.2	4.4	3.4	5	
11.0	11.6	12.3	11.9	10.5	11.8	11.9	0.7	13.1	9.9	6	
6.3	5.9	6.4	6.3	5.1	5.6	5.6	5.5	6.6	5.5	9	
6.8	6.7	7.4	6.9	6.0	6.7	6.6	6.0	7.3	6.2	10	
8.4	7.6	8.6	8.5	7.0	7.2	7.2	7.1	8.5	7.3	11	
16.5	17.4	17.3	16.3	19.5	17.9	18.3	12.7	18.3	16.8	12	
1.7	1.9	2.0	1.8	2.7	2.1	2.1	1.4	1.8	1.8	13	
1.4	1.7	1.5	1.4	2.0	1.6	1.6	.9	1.5	1.5	14	
18.1	19.1	18.1	27.0*	14.1	14.0	15.6	14.0	19.0	14.5	15	
										I_{IH} Max - 40uA	
			*Continues to rise with voltage applied								

TABLE 7-I (cont.)

NOTE: All readings within 1uA of those at 4.5V except as noted.

SN31	SN32	SN33	SN34	SN41	SN51	SN52	SN54	SN61	SN62	V_{CC} = 5.25V Pin Number	Meas.
										1	I_{IH}
										2	
										3	
										4	
										5	
										6	
										9	
										10	
										11	
										12	
										13	
										14	
			38uA							15	
										I_{IH} Max = 1.0mA	

TABLE 7-I (concl)

SN31	SN32	SN33	SN34	SN41	SN51	SN52	SN54	SN61	SN62	V_{CC} = 5.25V Pin Number Meas.
39.7mA	40.7	41.6	40.7	49.9	43.2	42.7	46.4	40.3	40.7	16 I_{CC}
										w/AE=high
										I_{CC} Typ=100mA
69.3mA	84.0	85.7	81.2	86.5	93.2	92.6	71.4	68.9	50.8	16 I_{CC}
										w/AE=low and
										LE=high
										I_{CC} Typ=9.0mA
.3uA	.3	.1	.1	.5	.8	.8	.3	.1	.7	7 I_{off}
										2.4V
										I_{off} Max = 100uA
-.2mA	-.3	-.1	-.1	-1.3	-.8	-.3	-.3	-.i	-.8	7 I_{off}
										0.5V
										I_{off} Max = 50uA

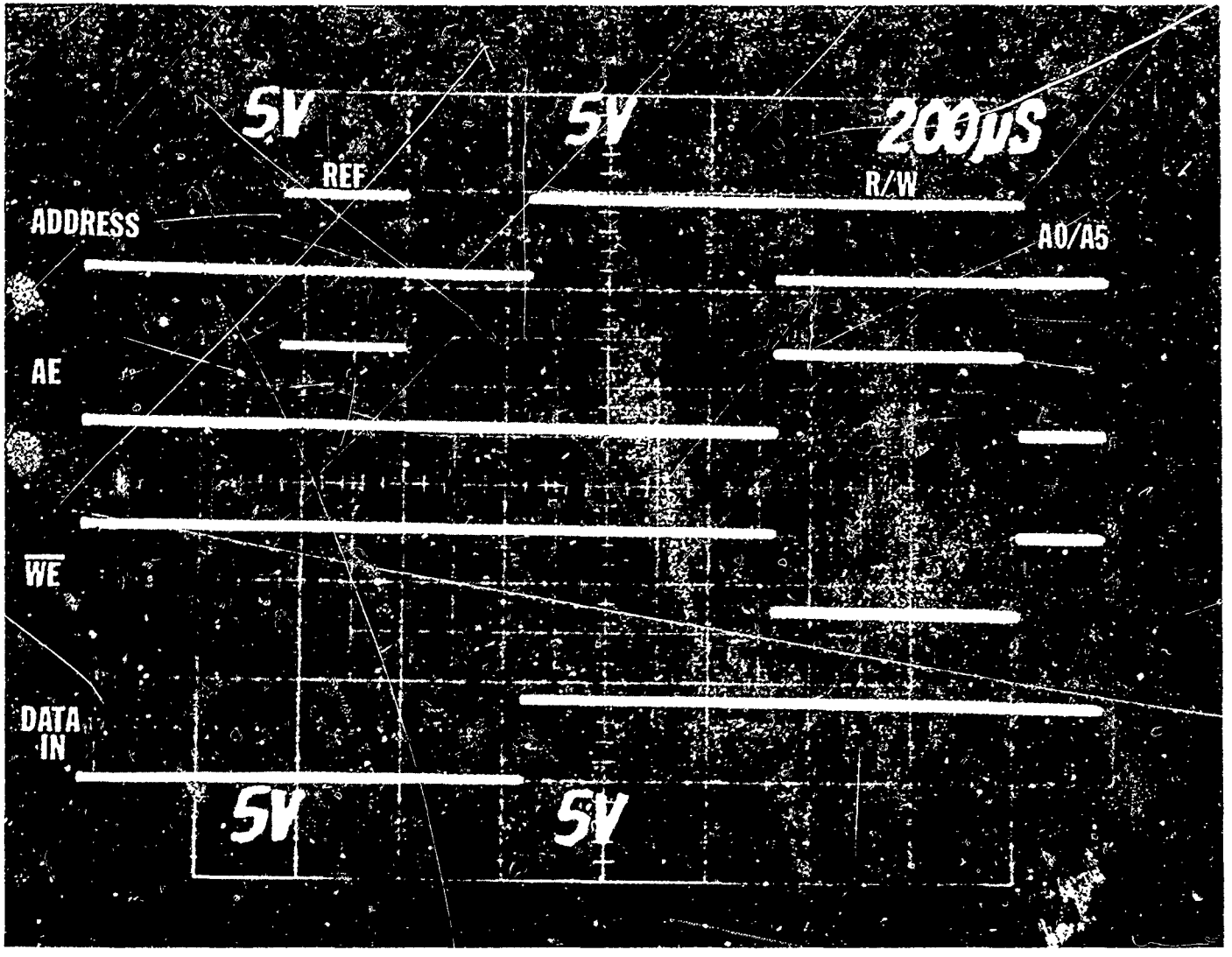


Photo 7-1 Four Typical Waveforms Provided By the Functional Test Circuit for Testing the Bipolar 4096 Bit Dynamic Ram.

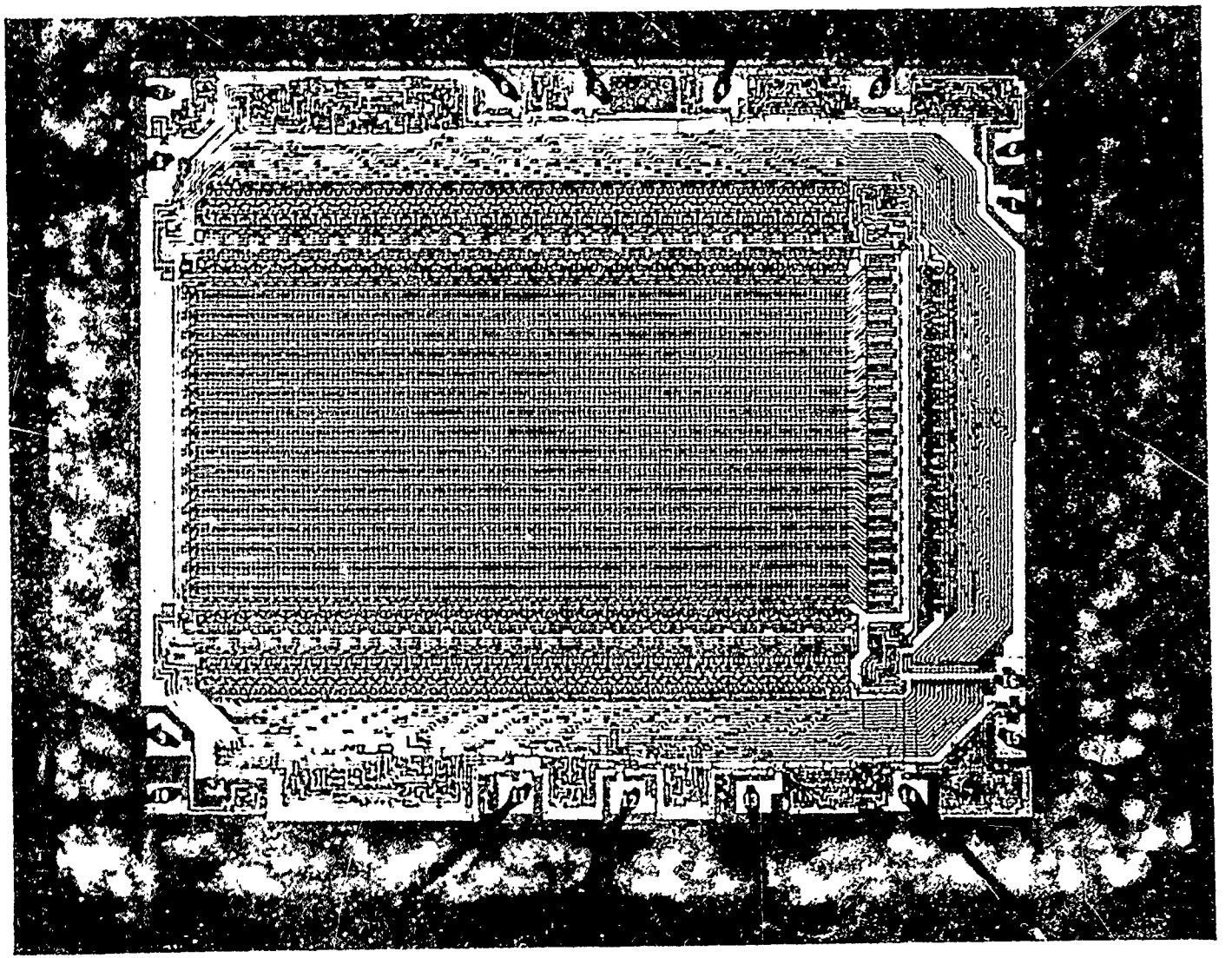


Photo 7-2 The Complete Die, Mag. - 40X

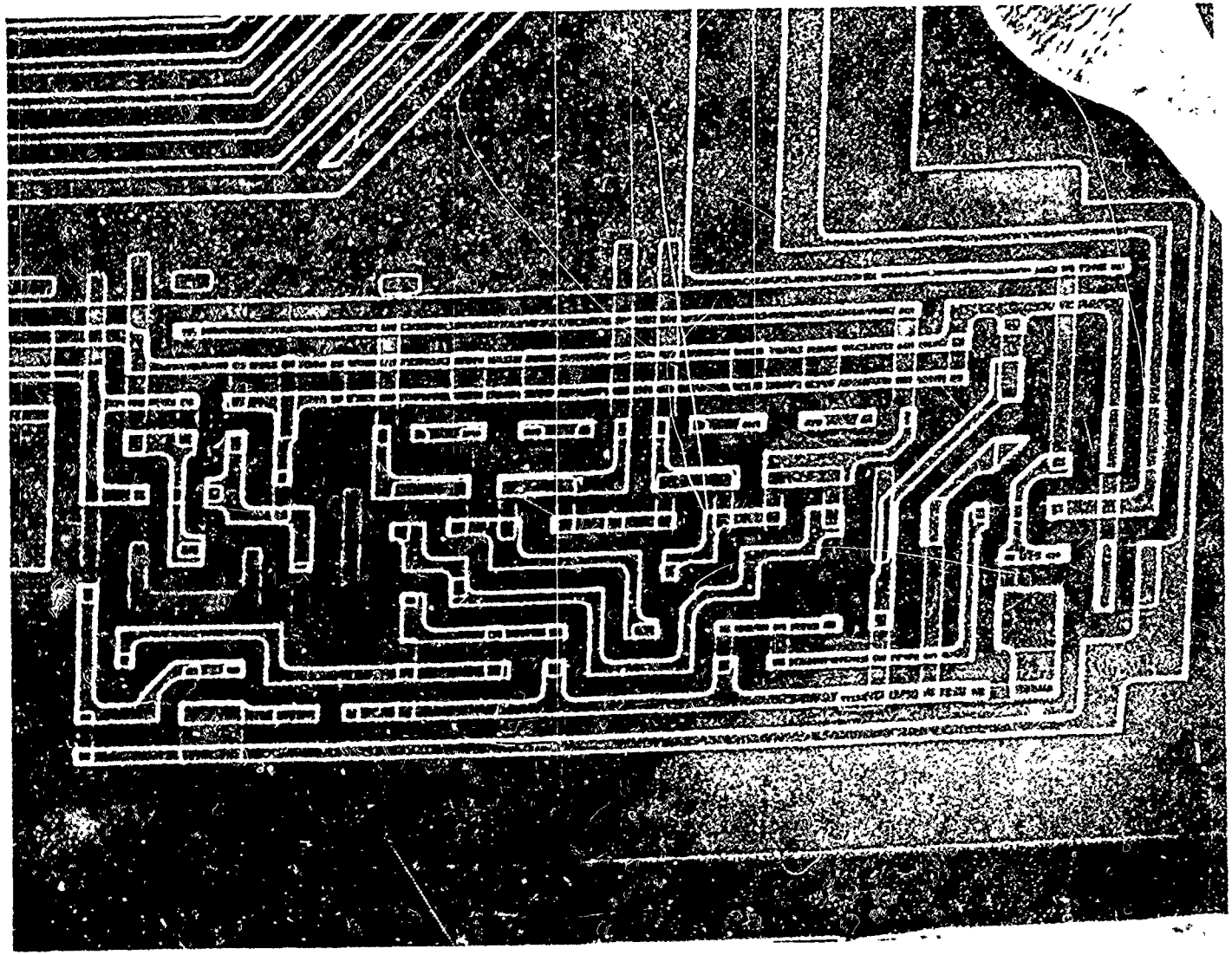


Photo 7-3 A Secondary Electron Image of the A0/A1 Row and Column Address Buffer and Encoder Circuit. 15 KV, Mag. - 460X

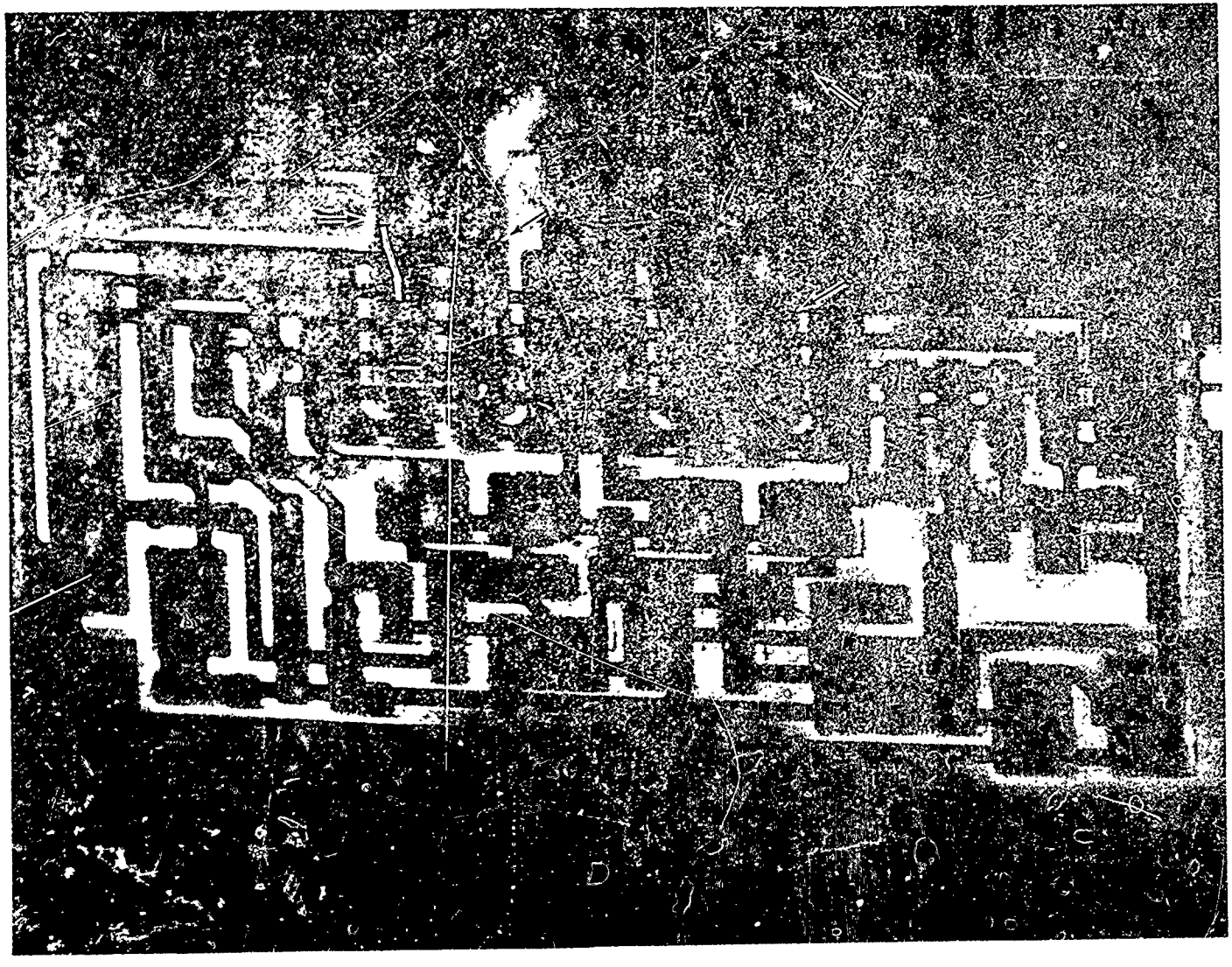


Photo 7-4 EBIC Micrograph of Same Area as Photo 7-3. Arrows Locate Buried Layer Interconnects at Buffer Output. 15 KV, Mag. - 460X

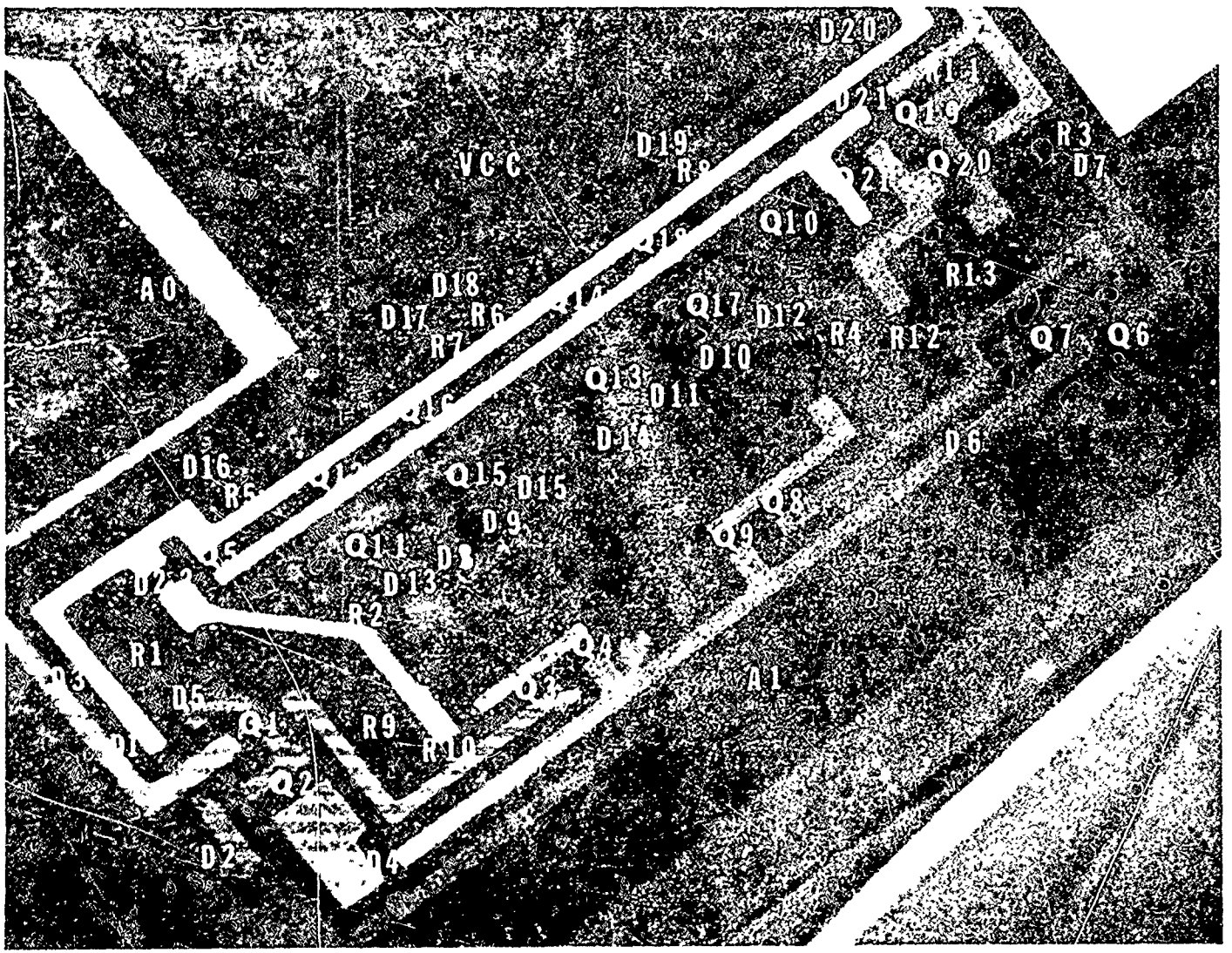


Photo 7-5 Voltage Contrast Micrograph of the A0/A1 Row and Column Address Buffer and Encoder Circuit. 1.2 KV, Mag. - 460X

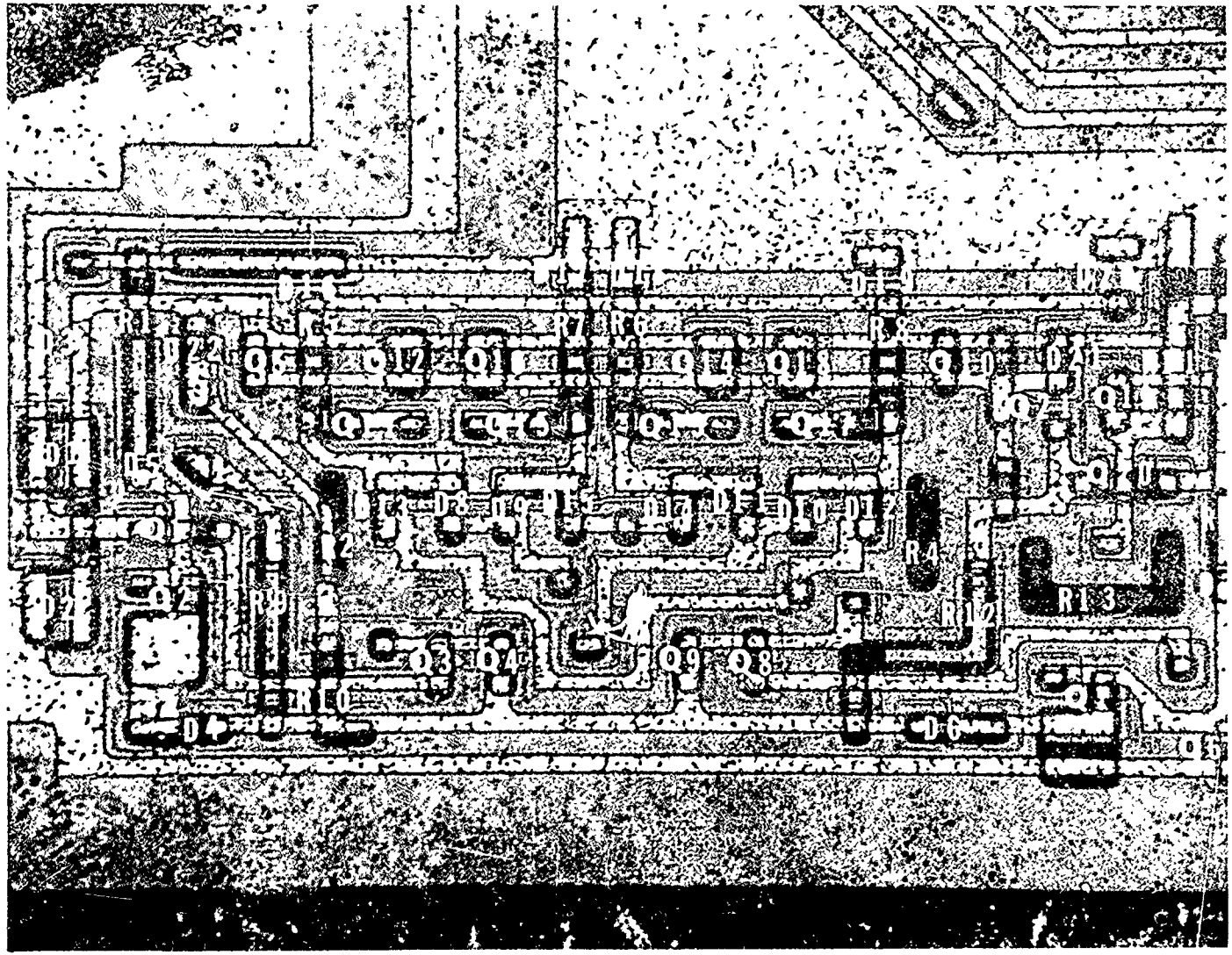


Photo 7-6 Light Photograph of the A0/A1 Row and Column Address Buffer and Encoder Circuit. Mag. - 460X

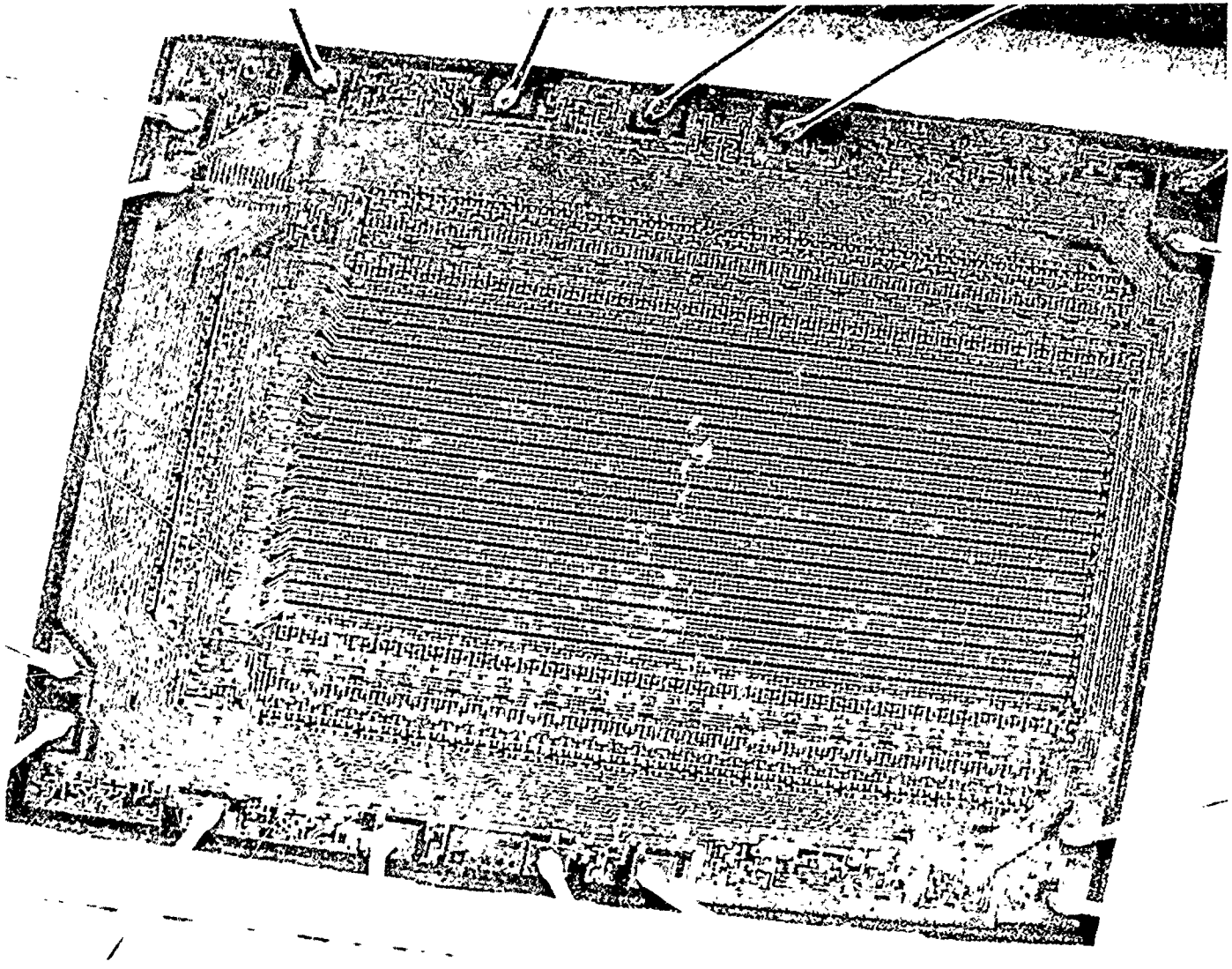


Photo 7-7 Secondary Electron Image of the Complete Die. 15KV, Mag. - 45X

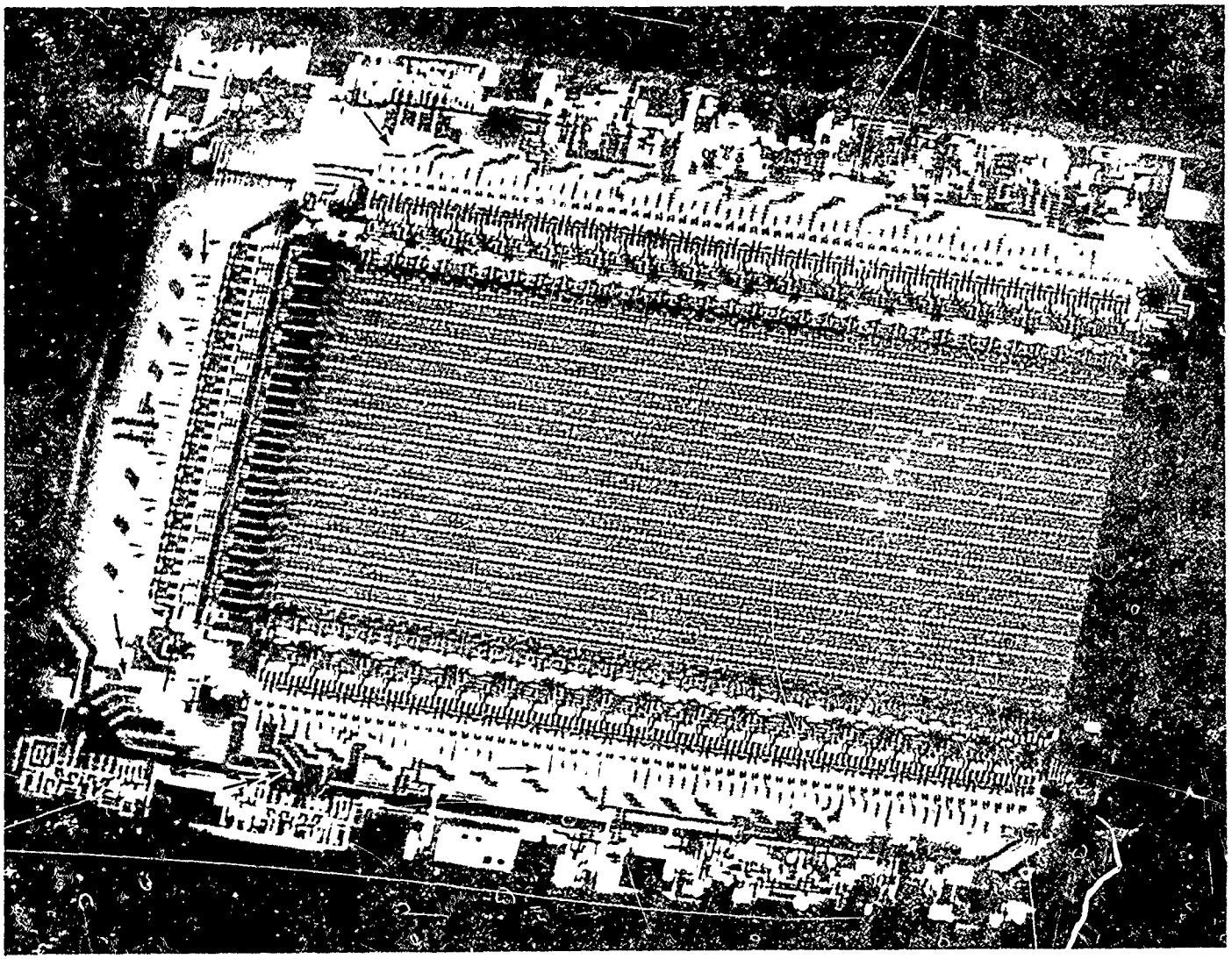
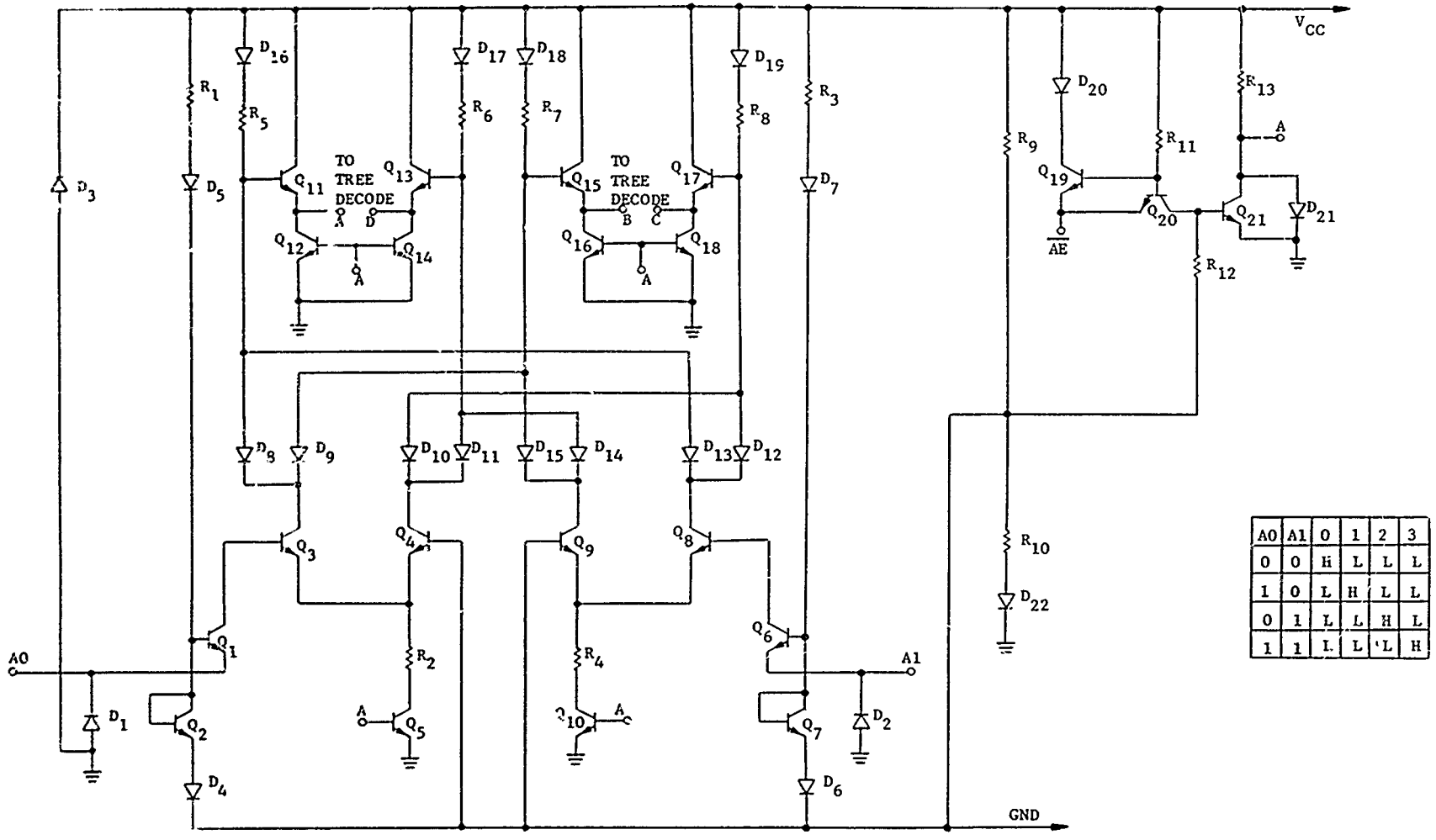


Photo 7-8 EBIC Micrograph of the Complete Die. Single Arrows Locate Buried Layer Interconnections With Tree Decode Inputs. Double Arrows Locate Buried Layer Interconnections With Address Buffer Outputs. 15 KV, Mag. - 45X



A0	A1	0	1	2	3
0	0	H	L	L	L
1	0	L	H	L	L
0	1	L	L	H	L
1	1	L	L	L	H

Figure 7-1 Schematic, Row and Column Address Buffer and Encode

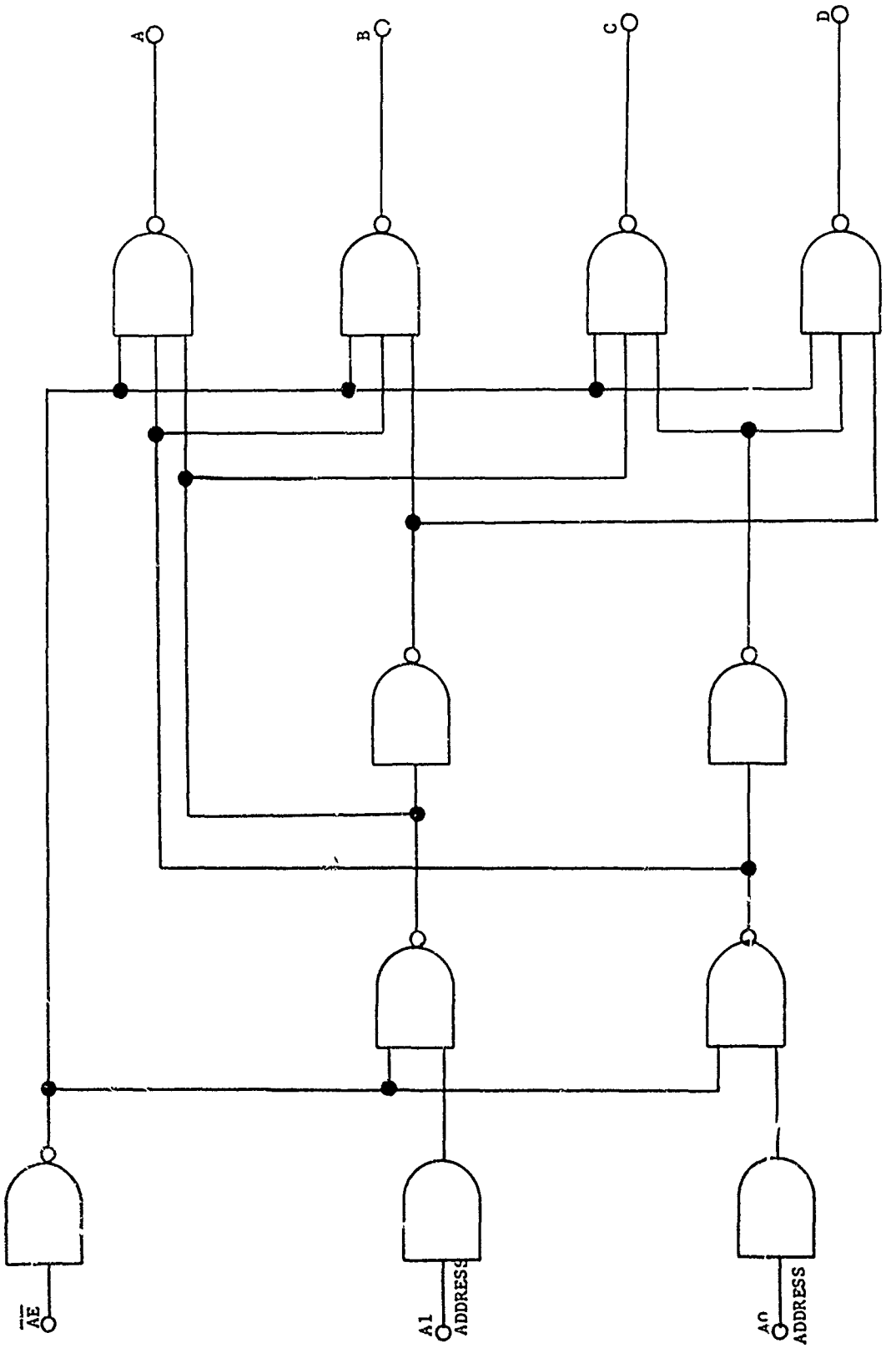


Figure 7-2 Row and Column Address Buffer and Encode Logic Diagram

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4.8 SUMMARY

The characterization of the seven types of memory circuits was very successful. SEM application techniques were developed and demonstrated which complemented light optic techniques. The practicality for using these combined techniques was verifed for complex LSI circuits.

The primary problem encountered during this study was the removal of glass passivation and maintaining functional operation of the circuit. This is a major concern because it presents a high risk for failure isolation in failed circuits. There is a high probability that the failed circuit may be damaged or degraded during passivation removal. This is a risk which generally cannot be tolerated because each circuit failure is usually unique. Removing glass passivation is a complex problem. A wide variation in glass passivation chemistry was experienced on devices with different date codes. This further complicates the problem with an additional variable. An etching procedure developed for a specific part may not produce consistent results because of these glass variations.

It is very likely this risk could be significantly reduced by a different etching procedure. There are two basic problems with wet chemical etching, maintaining surface cleanliness and limiting the attack on metallization. Experience to date shows that gas plasma etching is a very promising technique. Limited evaluations were conducted in parallel with this study. The problem experienced with plasma etching is that current gas mixtures produce higher etch rates for doped silicon than they do for silicon oxides. If a heavily doped silicon diffusion is exposed to plasma etching by little more than a pinhole, a major portion of the diffusion is etched away which results in electrical failure. Further investigation is planned to try and resolve this problem.

Functional mapping was shown to be very effective for characterizing both static and dynamic memory circuits. It provides valuable insight into circuit operation. Signal and clock lines are easily identified and internal circuit interfaces are quickly located. Functional mapping is a key factor in providing practical characterization of complex circuits.

EBIC was shown to be impractical for silicon gate NMOS circuits. These circuits are unable to tolerate the irradiation damage produced by the electron beam. EBIC evaluation was attempted using the minimum acceleration voltage needed to penetrate the surface. This was not successful. A similar problem has been experienced on silicon gate CMOS circuits. The beam irradiation appears to produce a residual charge in the gate oxide causing the device to remain in conduction. EBIC was shown to be valuable for evaluating bipolar and metal gate MOS circuits. It provides supplemental diffusion data for correlation with other circuit data. EBIC has been shown to be mandatory in developing circuit schematics for I^2L circuits. It is currently the only technique which is capable of locating buried layer interconnections.

The SEM application techniques have demonstrated their value in isolating circuit failures. It appears to be the most practical approach that is

currently available. Application can be limited by the glass passivation removal procedure which is currently available. It should also be pointed out that glass passivation removal is generally required for other failure isolation techniques. Therefore, this limitation is one of general concern.

5.0 SEM OPERATING GUIDELINES

5.1 SPECIAL CONSIDERATIONS

These special considerations are intended to provide additional insight regarding SEM operation. These considerations are limited by the experience from the devices evaluated and utilization of a single SEM instrument. It is likely that problems will arise that are unique to circuits or instrumentation and which are not described in this report. These problems can best be solved by identifying the major parameters and conditions which influence the problem. Evaluate each factor to determine which is the most significant. Beginning with the most significant factors identify what changes can be made to reduce their significance.

Consider image signal to noise ratio as an example. The major parameters would include:

- Electron Beam Current;
- Imaging scan speed (video band pass);
- Sample charging;
- Secondary electron detector sensitivity.

In reviewing this list the first response may be to increase the beam current. This could help a signal to noise problem but may more severely increase a surface charging problem. The recommended approach is to evaluate each parameter by changing the variables associated with them and measure the results. What effect is realized if the beam current or scan speed is increased or decreased? Is there anything around the sample which may contribute to charging and thereby reduce secondary electron access to the detector? Can any improvement be realized by shielding the sample and test socket assembly? What effect is realized by increasing and decreasing the beam acceleration voltage while maintaining the same beam current? Can the secondary electron detection efficiency be improved by closer location to the sample or by using a more sensitive detector material? Each of the responses for these factors will vary for different instruments and circuit interface schemes. Most important is to determine what this significance is and what advantages or compromises must be considered. The objective is to optimize these factors to obtain the best performance. Once this optimum performance is obtained, document the parameters so it can be reproduced at a later time. Don't become inflexible as different technologies or device packages are encountered. It may require another appraisal to again determine the significance of the major parameters.

5.1.1 SURFACE CHARGING

Surface charging can be a very complicated problem because there are so many factors which can influence it. The effect of surface charging on voltage

contrast sensitivity is more severe than its effect on image resolution. Beam induced charge accumulation in a circuit oxide can completely mask voltage contrast from the underlying circuit. Charging of adjacent surfaces also interferes with the circuit voltage modulation of the secondary electron signal.

Adjacent surface charging was evaluated to determine how it might best be controlled. The most apparent method of control would be by the application of an evaporated conductive film. This was not utilized as it would provide circuit leakage paths which could degrade operational performance and it would compromise EBIC evaluation of the circuit. No practical way was found to apply a film without introducing these leakage paths. Another method would be to place a conductive "hat" over the circuit. A cover was constructed using aluminum foil which completely covered the device and socket. An opening was made in the top to expose the package cavity and circuit chip. The cover rested on the top of the package so the secondary electron trajectory was not significantly increased or impeded. There were two reasons for evaluating this cover, surface charging, and interconnect shielding. It was possible that power and signal lines servicing the device could produce interference fields. Evaluation of voltage contrast sensitivity and imaging showed no discernable difference with the cover installed or removed.

Another important factor is to avoid beam landings directly on nonconductive surfaces of the package. This results in a concentrated charge becoming trapped on the surface. Should this occur the surface will generally discharge quickly by returning it to atmosphere. If this is unsuccessful the part can be rinsed in alcohol and dried.

Beam induced charge accumulation in circuit oxides is the most significant problem to voltage contrast. This is due to the proximity of the oxide to the circuit voltage nodes and the oxides exposure to direct beam landings. Indications of oxide charge accumulation is the gradual visual fading of circuit voltage contrast. Also the effects of this charging can be seen by reducing the SEM scan magnification by 50% to 75%. The area scanned at the higher magnification will appear to be brighter or darker. (Note: A dark area produced by a net positive charge should not be confused with a dark area produced by surface contamination). Also the time required for this bright or dark area to dissipate is an indication of the severity of charge accumulation. Under very severe charging conditions the charge may not be dissipating but instead the surrounding area is charging up towards it. This can be determined by decreasing the magnification a second time to determine if a bright or dark area is again apparent. This charging condition is best observed using a TV or fast scan rate. Each time the scan area is increased (magnification decreased), the beam current or charge density over a given area is decreased. Therefore more severe surface charging occurs at higher magnifications.

Oxide charging can be reduced in a number of ways. The most significant factor is beam acceleration voltage. As the acceleration voltage is decreased, the number of emitted electrons approaches the number of incident

electrons at the surface. Stated in another manner the net negative surface charge decreases. This will continue until surface equilibrium is reached; i.e., the net charge is zero. Equilibrium reportedly occurs at two acceleration voltages. One is in the area of several hundred volts and the second lies between 1 and 10 KV. Between these two points of equilibrium the net surface charge is positive; i.e., the number of emitted electrons (secondary and backscattered electrons) exceeds the number of incident beam electrons. This is the operating region utilized for the silicon gate NMOS circuits which were examined with a 1.0 to 1.5 KV beam.

A second approach is to utilize an acceleration voltage where the electrons just penetrate the oxide. Good voltage contrast sensitivity can be obtained with relatively thick (0.5 to 1.0 um) passivation present. This is the approach used for bipolar and metal gate MOS circuits examined with a 5 KV beam. The compromise is possible irradiation damage. Some reasonable voltage contrast imaging has been accomplished on bipolar and metal gate CMOS circuits, without removing the glass passivation.

For silicon gate MOS circuits and bipolar and metal gate MOS, if beta or threshold degradation is a concern, the 1.0 to 1.5 KV beam must be used. For bipolar and metal gate MOS circuits where some beta or threshold degradation is tolerable; e.g., schematic development, the 5 to 10 KV beam can be used.

A third approach to reducing surface charging is by reducing the beam current. Reducing beam current requires a compromise between surface charging and image signal to noise ratio. Lower beam currents were found to be necessary for 1 KV operation as compared to 5 KV operation.

Another factor in reducing surface charging and improving voltage contrast is to reduce the glass passivation thickness. Two visual indications that were used to evaluate satisfactory reduction of the passivation thickness are the presence of dc voltage contrast on metallization, and the ability to obtain ac voltage contrast response from underlying circuit diffusions. This second indicator was not practical to obtain for I^2L and some MOS circuits.

5.1.2 ELECTRON BEAM/CIRCUIT INFLUENCE

During this study there were no observed instances where the elecron beam influenced or controlled a circuit state. This would be expected to occur at higher beam voltages and currents where significant currents can be injected into circuit nodes. These injected currents could produce conduction states which result in abnormal circuit operation. This typically is observed where a circuit operates differently with the beam on and off or where the observed circuit function changes between two scan magnifications. The only beam effects observed in this study were fixed changes which resulted from beam irradiation damage. These were changes where MOS transistors remained in conduction after the beam was removed and after the device was removed from the SEM. Sometimes these circuits could be recovered using high temperature anneal. Another beam affect was the erasure of the memory program in an EPROM circuit. The programmed data was lost

when this circuit was exposed to a 3 - 4 KV electron beam. This beam exposure removed the injection charge on the floating gate elements. Reprogramming after electron beam erasure was successful.

5.1.3 OPERATING MODES

The sample tilt angle used during this study ranged from 5 to 10 degrees. This tilt angle was selected to provide compatibility with voltage contrast and EBIC imaging. The best EBIC imaging is obtained with near perpendicular beam incidence. In EBIC, the target is the detector and large sample tilt angles reduce the definition for vertical junctions. The 5 to 10 degrees of tilt results in some loss in secondary electron yield. This was considered to be an acceptable tradeoff for providing SEI and EBIC imaging without the need to change the tilt angle and reposition the sample.

One of the major criticisms of functional mapping is that the circuit is observed while operating at an abnormally low frequency. The key purpose of functional mapping is to display circuit operation for interpretation. It has been demonstrated to satisfy this need extremely well. A special technique was developed for applications where circuit operation is required at more typical operating frequencies. This technique combines the advantages of stroboscopic beam blanking and functional mapping. A candy stripe voltage contrast pattern is provided in a single photograph with the circuit operating at frequencies up to 1-2 MHz. Voltage contrast micrographs of circuits operating above 100kHz had to be taken directly off the visual CRT. The reduced frequency bandwidth through the record CRT video channel will not pass the high frequency chopping component at the higher blanking frequencies. Photo 5 is a voltage contrast micrograph which was taken at a frequency of 1.4 Hz and using a 5 KV beam. Photo 6 is a voltage contrast micrograph taken under the same conditions except the circuit is operating at 40 kHz. The only difference between these photos is a slightly discernable high frequency artifact in Photo 6. This technique requires the capability of beam blanking on the SEM. The logic diagram for the control circuit is shown in Figure 3. This circuit utilizes five sychronous 4-bit up/down counters as dividers. Switch 1 selects the frequency equivalent to the operating frequency of the circuit function being examined. This switch provides a binary division from the clock input of up to 32. Switch 2 and a patch matrix selects the period or voltage contrast stripe width on the displayed image. This provides a binary division from the clock input. This division is used to reduce the clock frequency to 1 - 2 Hz. The line driver circuit used is the same as used in Figures 1 and 2. Sychronizing the input clock frequency with the SEM line scan improves the stripe sync over various clock frequencies. Beat frequency patterns will appear at harmonic frequencies between the clock and SEM scanning frequencies.

The complete circuit provides beam strobing of the displayed circuitry whenever the input is high for one stripe width period. During the second stripe width period, the beam strobes the circuit whenever the input is low. Beginning with the third stripe width period the strobe versus signal phase continues the alternating sequence. This produces an image which contains alternating circuit states. This image is similar to the low frequency functional map except for two differences. One is the operating

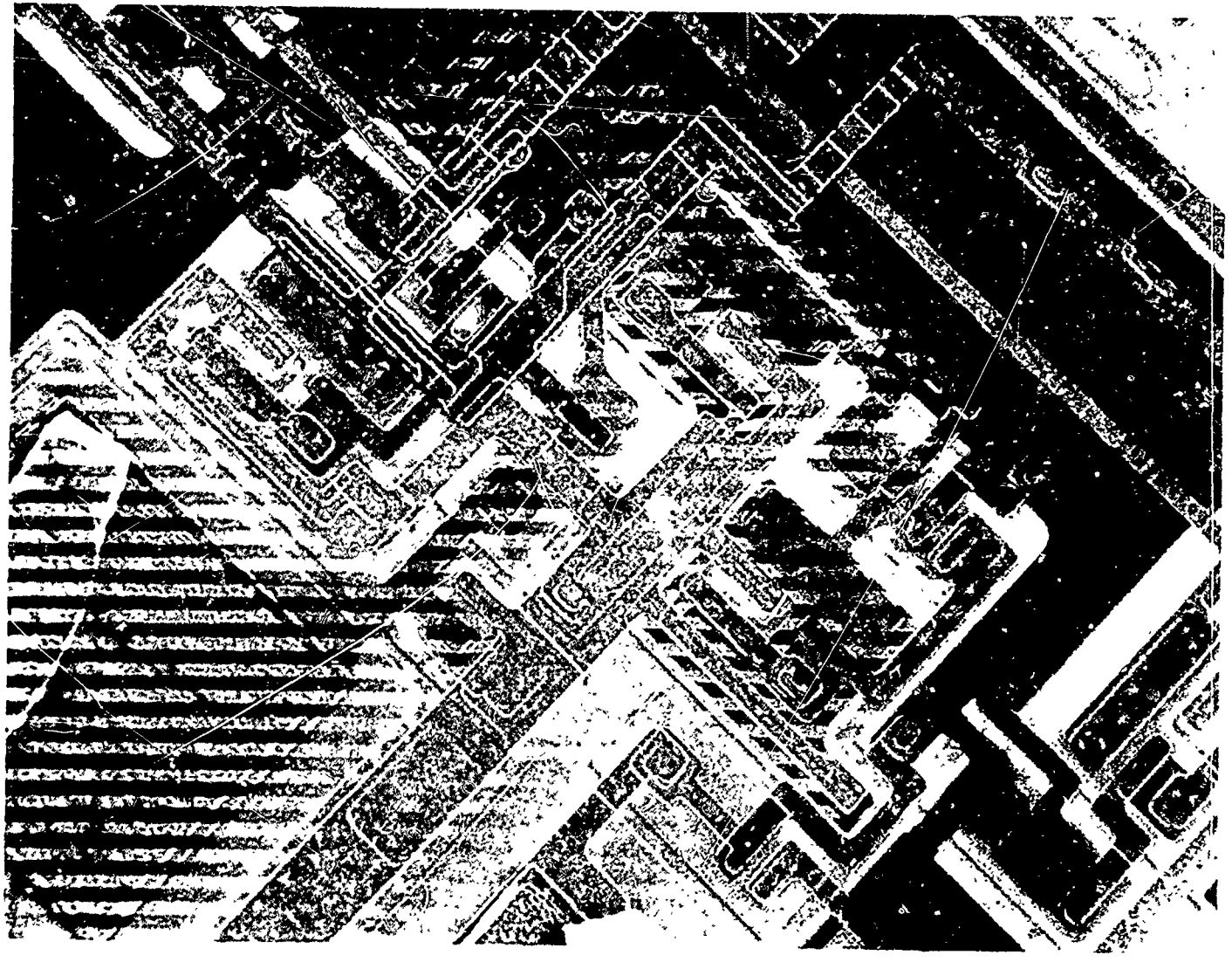


Photo 5 Voltage Contrast Micrograph Showing Funcrional Mapping at 1.4 Hz. 5 KV, Mag. - 500X

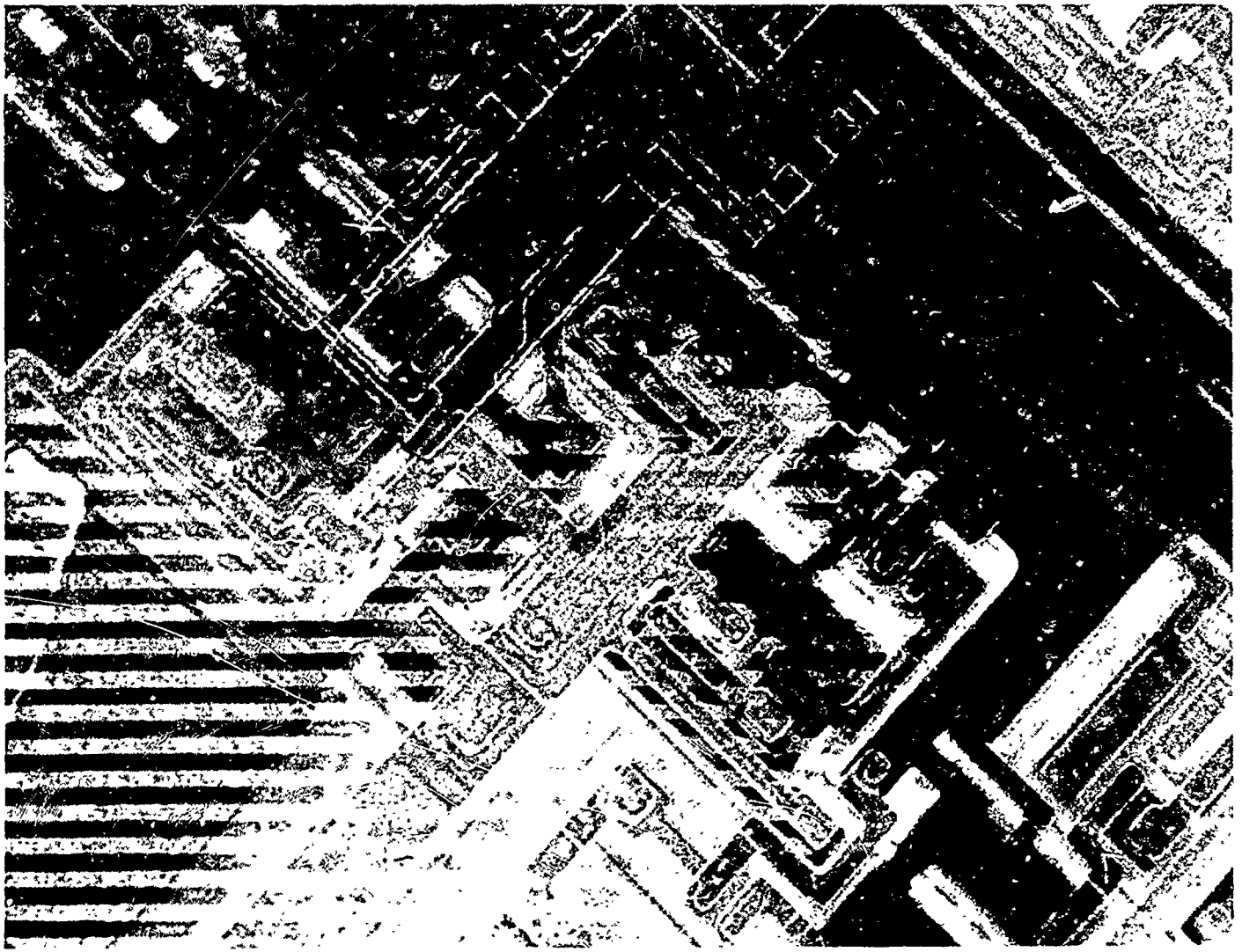
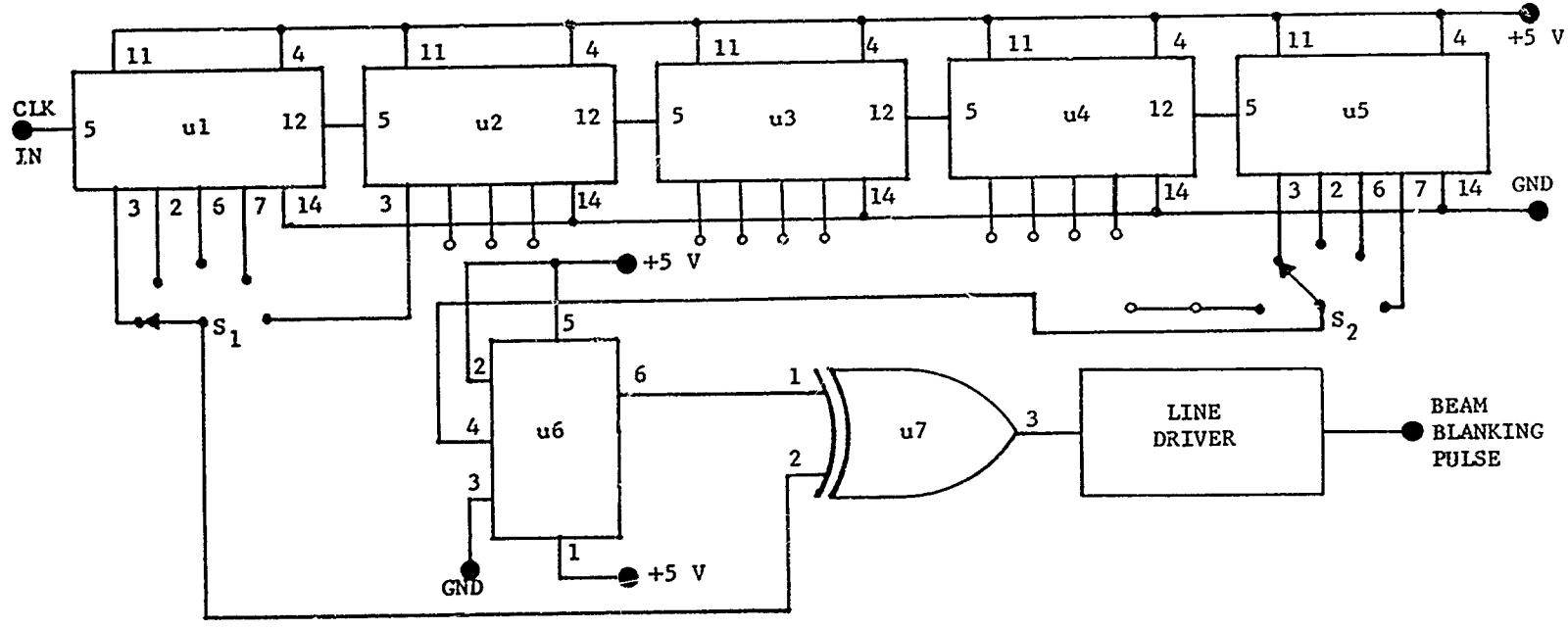


Photo 6 Voltage Contrast Micrograph Showing Beam Blanked Functional Mapping at 40 KHz. 5 KV, Mag. - 500X



Sym	No	V_{CC}	GND
u1	74193	16	8
u2	74193	16	8
u3	74193	16	8
u4	74193	16	8
u5	74193	16	8
u6	74109	16	8
u7	7486	14	7

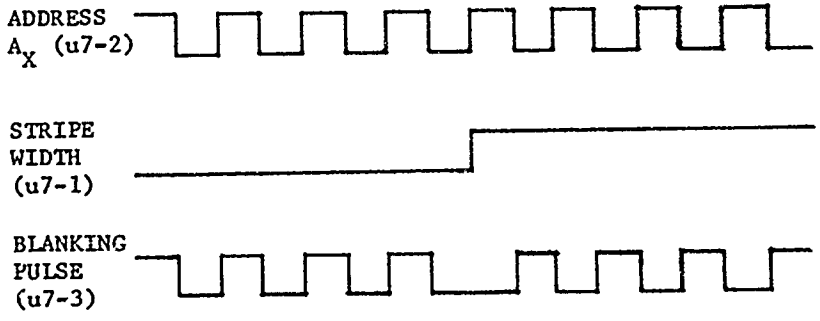


Figure 3 Beam Blanked Functional Mapping Circuit.

frequency of the circuit and second the beam blanked functional map can only display voltage contrast striping for a single circuit operating frequency. Beam blanked functional mapping was not used during this study because the higher circuit operating frequencies were not required and special emphasis was placed on the use of a basic SEM instrument.

5.2 RECOMMENDED OPERATING GUIDELINES

There were no extraordinary SEM operating procedures used in evaluation of the devices during this study. The SEM operating procedures used are representative of those utilized for obtaining high quality imaging. Prior to activating the beam, adequate time should be allowed to obtain sufficient evacuation of the specimen chamber. This will reduce the formation of hydrocarbon film contamination. This contamination reduces secondary electron emission and acts as a mask during subsequent passivation etching. Contamination masking is discussed further in the device preparation section of the device characterization procedure. The specimen chamber vacuum used during this study ranged from 5×10^{-6} to 1×10^{-6} torr.

The electron source used was a tungsten filament biased to provide 250 ua of emission current. A lanthanum hexaboride (LaB_6) electron source was evaluated for performance comparison. LaB_6 rod electron emission was generated through the combination of radiant and electron bombardment heating. The primary LaB_6 advantage of increased resolution at low acceleration voltages was not needed because voltage contrast imaging is performed at low scan magnifications. The performance of the LaB_6 and tungsten sources in voltage contrast was found to be comparable.

The electron beam acceleration voltages were basically confined to the area of four voltages; 1, 5, 10, and 15 KV. These beam voltages were selected on the basis of specific application performance. The 10 and 15 KV beams were used for secondary electron and EBIC imaging of bipolar circuits. The 1 and 5 KV beams were used for voltage contrast imaging of silicon gate MOS and bipolar circuits. The electron beam currents are measured using a faraday cup. The beam currents used for the 10 and 15 KV beams were in the 100 to 200 pA range. The beam currents used for the 5 KV beam were in the 200 to 500 pA range, and the beam currents used for the 1 KV beam were in the 25 to 50 pA range. The 10 and 15 KV beam currents used are typical for routine applications in this acceleration voltage range. The 5 KV beam currents used are higher than typical for routine applications. These beam currents would typically be in the 100 - 200 pA range. Higher currents were used to improve the signal to noise ratio for imaging at TV scan rates. The decreased resolution which occurs at higher beam currents was not a factor because low magnification imaging is used. Also the increased beam current did not produce a surface charging problem. The 5 KV beam provides sufficient penetration of the surface oxide films to increase their conductivity and thereby eliminates serious surface charging. The 1 KV beam currents used are less than typical for routine applications. It was determined that these beam currents were required to sufficiently reduce surface charging for acceptable imaging. The increased signal to noise ratio for imaging at TV scan rates was considered to be tolerable at best (Note: The SEM instrument used in this study provides TV scan rates on the visual CRT.

This CRT has a slow phosphor which reduces the apparent noise in the displayed image). These acceleration voltages and beam currents were arrived at on the basis of the needs for the respective applications. This was accomplished on the basis of trial evaluations.

The secondary electron detection and imaging circuit used is the standard configuration supplied in this instrument. The secondary electron detector is a phosphor coated quartz light guide. This detector provides significant improvement in detection sensitivity and performance life as compared with the metallized plastic scintillator detector. The longest light guide length was used to position the detector as close to the target as possible.

The sample current amplifier used for EBIC amplification and imaging is also a standard configuration supplied in this instrument. EBIC signal steering is accomplished using the switch matrix developed expressly for this purpose. This interface is described in the device/SEM interface section of this report. The EBIC levels obtained from the evaluation device circuits ranged from 10^{-7} to 10^{-9} amps.

The imaging scan rates are best selected by operator preference. All SEM photographs were taken using a 60 second frame and 800 lines/frame. All photographs contained in this report were processed using Ektopan 4 x 5 negative film which has an ASA 100 rating. This film provided the needed resolution and contrast for report reproduction. The 8 x 10 photo size was used to provide adequate visibility of detailed circuitry. No video signal contrast enhancement was used during negative film exposure with exception of the I^2L voltage contrast photo.

6.0 DEVICE CHARACTERIZATION PROCEDURE

These procedures are based upon the methods used and the experience gained during this study. It is intended to provide the analyst some basic insight and guidance for performing circuit characterization. The quantity of devices needed for characterization ranged from 5 to 10 devices. Of these, 2 to 5 devices were electrically good devices and the remainder were mechanical samples from the same lot date code. The larger number of good devices was required where difficulty was experienced in successfully removing glass passivation.

6.1 DEVICE PREPARATION

Each device used in developing characterization data is parametrically and functionally tested to verify proper operation. Parametric testing is performed only for this initial test. The parametric retesting is not performed after initial testing because it does not provide a representative measurement of the total circuit. Functional testing provides a more representative measure of the complete circuit, even though it is less sensitive to parametric changes. It is very likely, and in some cases certain, that internal circuit parameters are degraded during glass passivation removal. Functional verification of proper circuit operation is important, because visual circuit operation is utilized in developing and verifying the electrical schematic. All device packages can be opened by thinning the

metal or ceramic lids using a grinding wheel. The metal lids are thinned to the point where they exhibit "oil canning." This grinding is performed using 400 grit silicon carbide paper. The ceramic lids are thinned using a 70 micron diamond impregnated wheel. Care should be taken not to break into the package cavity during grinding. A sharp tool is used to penetrate the thinned lid using care not to damage the wires or die. If cleaning is required an effective method is to use Transene* ultrasonic detergent. The device is dipped (one second exposure) into the sonicated detergent solution. It is then rinsed in DI water followed by isopropyl alcohol and lightly blown dry with dry nitrogen (Note: This short exposure to ultrasonic cleaning has not resulted in die or wire damage). Following decap the device operation is verified by functional testing.

The glass passivation is removed using wet chemical etching. A glass etching evaluation is performed on each part type using mechanical samples or partially functional circuits. This is necessitated by the wide variation experienced in etch rates between device types. The bipolar circuits typically show a greater tolerance to wet chemical etching. There are two etchants which produce good results:

Number 1		Number 2	
125 ml hyudrofluoric acid	48%	280 ml ammonium fluoride	40%
25 ml nitric acid	70%	35 ml hydrofluoric acid	48%
250 ml glycerine			

Etch No. 1 is satisfactory only for bipolar devices and etch No. 2 is satisfactory for all devices. The etch rates are dependent on the type of deposited glass and chemistry (Note: Experience shows that etches having high glass etch rates produce obvious grooves immediately adjacent to the metal conductors. This results in premature removal of the thermal oxide, aluminum etching, and deterioration in functional performance.)

The glass removal is evaluated using 30 second etchant exposure, wash in DI water for 30 to 60 seconds, rinse in isopropyl alcohol and gently dry with dry nitrogen. The etching progress is monitored by light microscopy. The die is observed for the appearance of vivid oxide color which is characteristic of the thermal oxide. Also the exposed aluminum at the bond pads and the metal conductors are checked for indications of damage and undercutting. Following each etch exposure a simple functional test is helpful to verify circuit operation. A good indicator is to track the V_{CC} or V_{DD} supply current. Any change generally signifies that further etching will not be tolerated by the circuits. When it appears sufficient glass has been removed, the next check is to evaluate the voltage contrast performance in the SEM. The two criteria to observe are dc voltage contrast for metal conductors and ac voltage contrast for diffusions. This is also an opportune point to optimize the beam operating parameters. Once the die surface has been examined in the SEM, a film of contamination is deposited on the surface. This film should be removed prior to additional etching, so it

*Transene Company, Inc. Rowley, MA

does not act to mask these areas during subsequent etching. This film is easily removed by oxygen plasma. Typical exposure time is 5 - 10 minutes. The etch evaluation should determine four factors; etchant, approximate etch time, oxide color appearance required for satisfactory voltage contrast and optimum beam operating parameters.

A functionally good sample is then prepared using these evaluation data and following the same procedure. If the evaluation data indicates 2 minutes of etch time is required it is recommended that the first etch exposure be half to three fourths of this time. Care should be taken to avoid over-etching the device.

This is a good point to take an overall light photograph of the die. This photo is helpful in finding locations during SEM evaluations.

6.2 CIRCUIT EXCITATION

The test sample is placed in the SEM and the required address and timing signals are applied. It is helpful to observe the total device in operation with a low frequency (5 Hz) cyclic address pattern applied to the device. Observing the device image at a TV scan rate allows quick visual recognition of circuit functional blocks. This familiarity will be helpful in locating specific areas of the circuit as the characterization progresses.

Identify the primary functional address or clock signal. This can be determined from the device timing diagrams provided on the data sheet. This is the recommended starting point for developing the circuit schematic. Low frequency functional mapping is recommended for SEM evaluation. A square wave signal is applied to the primary signal line and it is recommended that secondary clock and address signals be pulsed. These signals can easily be provided by a word generator. The use of a reduced signal amplitude (0.5 volts above and below input threshold) on signal inputs will significantly reduce voltage contrast bleedover from adjacent interconnect wires.

The signal excitation frequency is an important factor affecting the object visibility. For example when the frequency is too low, the candy stripe pattern tends to segment the conductor stripe. This occurs when the contrast stripe width is much greater than the conductor width. When the contrast stripe width is equal or smaller than the conductor width the conductor is accentuated. The excitation frequency is selected in relation to the SEM frame used in photography. This relationship is identified by the following equation:

$$(1)\quad \text{Excitation freq} = \frac{\text{cycles per frame}}{\text{frame period (Sec)}}$$

The number of cycles desired per frame is dependent upon the image magnification and conductor stripe widths. A typical value would be 30 to 40 cycles per frame.

6.3 SEM EVALUATION

Utilizing the optimum SEM beam parameters locate the first circuit area to be examined. The area of interest can be easily located by exercising only this circuit. This operating circuit is readily located using the TV scan rate. To obtain a candy stripe pattern on the majority of the conductors, rotate the sample so that the scan axis intercepts the conductors at approximately 45° (Note: The sample can be physically rotated or the image can be electrically rotated). Photograph the circuit block using a 4 x 5 photo format. Verify apparent circuit operation by the presence of symmetrical voltage contrast striping on the circuitry. If practical take the voltage contrast, EBIC and SEI photos at this time. Take photos of adjacent areas and construct a montage if the complete circuit cannot be included in a single photo for the required magnification. Repeat this procedure for each functional circuit block.

6.4 LIGHT MICROSCOPE EVALUATION

Use the SEM voltage contrast photo to locate the circuit boundaries. Photograph the circuit using a 4 x 5 photo format. Black and white photos are satisfactory. If common diffusion identification by oxide color is required during schematic development, this is effectively accomplished by light microscope examination of the actual part; therefore, color photographs are not required. Should a quescion arise regarding interpretation of data in the photograph, use the microscope to examine the device at a higher magnification and verify the data. For example if a metal/diffusion connection cannot be determined in the photo it can easily be checked on the microscope. For complex circuits containing dense metallization it is recommended that the circuit be photographed without metal. This photo helps to simplify the location of circuit components. A glass passivation etch evaluation sample is a good candidate for this purpose. The metallization is removed using an aluminum etch. Repeat this procedure for each functional circuit block.

6.5 CHARACTERIZATION PROCEDURE

6.5.1 SCHEMATIC/DIE MAP

Utilizing all the SEM and light microscope photographic data, locate and identify the input, power and ground busses. Follow the input conductor and identify the circuit components. Draw these components and their interconnections in schematic form. Sequentially number the components on the photos and schematic as they are identified. Identify all components with connections common to a circuit node prior to proceeding to the next circuit node. Use the photographic data to identify the component terminals; i.e., base, gate, anode, diffusion polarity, Schottky junctions, etc. MOS circuitry that operates from a single 5 volt supply generally contains both enhancement and depletion mode FETS. These can usually be distinguished from each other by the termination of the gate terminal. The enhancement mode device has the gate terminal connected to drain and the depletion mode device has the gate terminal connected to source. These devices usually do not have any visually identifiable difference in appearance. Care must be

exercised during translation of the components and their connections onto the schematic.

When all components have been identified the schematic should be redrawn to improve visual interpretation. All power and signal interfaces should be identified. The standard format is input-left, output-right, power-top, and ground-bottom. Verify that the circuit operates as drawn. The voltage contrast photo can be used to check circuit operation. The photographic data is a valuable asset in developing the schematic and die map. When voltage contrast cannot be obtained; e.g., low level voltages in sense amp circuits, use the light photograph and EBIC photograph if available. Repeat this procedure for each functional circuit block.

6.5.2 LOGIC DIAGRAM

The logic diagrams are developed using the schematic data. The purpose of the logic diagram is to provide a simplified illustration of the circuits' function. The diagram should identify signal, data, and clock interfaces and depict their interdependence. It is helpful to include a truth table to better describe the circuit operation for complex circuits. A truth table should be included when there are four or more interdependent signals involved in a functional block. The logic diagram should utilize basic logic symbols; e.g., OR, AND, NAND, etc.

6.5.3 FUNCTIONAL BLOCK DIAGRAM

The functional block diagrams are also developed using the schematic data. The purpose of the functional block diagram is to provide a simplified overview of the total circuit. It should identify all the major circuit functions described by the schematic during characterization. Functional block interdependence is identified by an interconnecting line with an arrow depicting the direction of signal flow. Each block should be identified with the function title and all external device connections should be identified by point of connection, function and package terminal number. Power and ground terminals are identified by function and terminal only. Also it is helpful during future die examination to identify the functional block boundaries and package pin numbers on an overall die photo. These data are derived from the functional mapping photos taken during characterization. This allows the circuitry for each functional block to be located quickly.

6.5.4 BIT MAP

The bit map is developed by examing the functional operation of the die using SEM TV scan rate imaging. The row and column addresses are sequentially incremented to determine the row and column sequence for memory access. If access to memory rows or columns does not begin at one end and sequentially step to the opposite end, the address sequence is manually switched and the memory row or column access sequence is identified using the displayed SEM image response. The purpose of the bit map is to provide identification of individual cell physical location in the memory array by row-column address code. The address code sequence identification must be sufficiently complete to allow determination of each cells location.

This information is necessary for developing address patterns to evaluate test pattern sensitivities. There are a number of factors which relate to pattern sensitivities; e.g., location versus access time, location versus die thermal gradient, and intercell or interconductor crosstalk. The bit map is also invaluable in failure analysis for locating specific row and column decode circuits and related memory cells.

6.6 SUMMARY

These characterization procedures describe the evaluation sequence for memory circuits. They provide a practical approach to detailed circuit interpretation. It is recommended that if possible, the first attempt at characterization be performed using a static memory circuit. This would allow more concentration on establishing the procedural routines and determining the optimum instrument performance. The size of a static memory circuit is not a significant factor in determining the degree of difficulty for characterization. The larger the memory size the greater the repitition of each functional block. For example a memory circuit which has twice the memory capacity requires an additional row address buffer, column address buffer, and two times the number of decode circuits, sense amplifiers and memory cells. However, circuit characterization requires that only one circuit of each functional group be identified. The same duplication applies for dynamic memories except it includes a greater number of circuit functions that must be duplicated. The most significant are the circuit clocks. Therefore doubling the size of a dynamic memory does significantly increase the degree of difficulty. In all memory circuits the key factor that determines the difficulty of characterization is the density of the circuit. The higher the density the more difficult it is to interpret for schematic development.

7.0 FAILURE ISOLATION PROCEDURE

Device characterization is a valuable prerequisite for failure isolation. This provides needed familiarization with the circuit organization, physical layout and functional operation. This greatly increases the probability for successful failure isolation.

7.1 FUNCTIONAL TEST/FAILURE VERIFICATION

Functional testing plays an important role in failure isolation by helping to locate the functional area of the circuit where the failure resides. Prior to functional test it is recommended that the circuit be parametrically tested or evaluated by pin to pin curve tracer. This will identify any open or shorted circuit terminals.

The functional test signals should be verified to satisfy the specified timing requirements. Verification testing of an operational device is helpful. Perform a complete functional test on the failed device. Identify all address conditions which produce improper operation. RAM circuits should be tested by writing and reading various data patterns; e.g., all zeros, all ones, alternating 0, 1, and 1, 0. The testing should be sufficiently complete to identify all failure conditions.

Using the failed address conditions, develop the functional circuit possibilities which would cause this failure. For example do the failure conditions indicate commonality with a specific address buffer, row decode, column decode/sense amp, or output circuit. Test the circuit and verify the developed possibilities. A useful approach is to attempt to disprove these possibilities. This can sometimes lead to additional relationships and a better understanding of the failure. The time spent in functional test evaluation can significantly reduce the time required for failure isolation.

If the circuit failure cannot be verified it may be that the simulation conditions are incorrect. It is very important that these conditions be reviewed in conjunction with those reported at the time of failure. Two factors should be considered at this point; the failure may be an intermittent condition resident in the rejected circuit, or the failure may remain in the next assembly from which the rejected circuit was removed.

7.2 SAMPLE PREPARATION

The package should be opened using the same procedure identified in device characterization. Care should be taken to avoid damage to the failed part. Following decap and prior to any cleaning, perform a detailed microscopic examination. This should specifically include the examination of circuits implicated in the functional test evaluation. The examination should attempt to identify any evidence that may be related to the failure. It is recommended that anomalies be documented by photograph. It is important that the examination identify any conditions which may be affected by the glass passivation etch. An abbreviated functional test should be performed to verify the failure is still present. It is suggested that the device not be washed or cleaned unless the contamination present will interfere with the analysis.

It is recommended that consideration be given to attempt a SEM voltage contrast evaluation without removing any glass passivation. Successful evaluation and isolation has been accomplished in this manner for some bipolar and metal gate MOS circuits. This could reduce the chances of losing the failure. If it is unsuccessful it will be necessary to reduce the glass passivation thickness by etching.

The glass passivation is etched using the etchant and etch time guidelines developed during device characterization. It is advised to use care during glass etching by not attempting to remove too much glass during each etch step. Following each step the progress is monitored by microscopic examination. Also this examination should check for indications of attack on metallization, and following each etch exposure step the circuit should be functionally tested to evaluate the operational condition of the circuit and verify that the failure is present.

Failure isolation using SEM voltage contrast can be accomplished with a greater amount of glass present as compared with circuit characterization.

There is a compromise between increasing the chance of affecting the failure and the quality of voltage contrast imaging. The quality of the voltage

contrast must be considered the least significant. For example compare the characterization and failure isolation photos for the dynamic MOS RAM in this report. These failure isolations were made with more glass passivation present on the die. The primary objective is to isolate the failure with minimal effect or degradation on the failure or circuit.

7.3 FUNCTIONAL TEST/FAILURE VERIFICATION

The circuit is retested in a similar manner as performed during initial verification. This retest can be performed during sample preparation. The failure characteristics should remain the same as identified during initial failure verification testing. This is important as it is the only method which can be used to verify that the failure isolated is the original failure. The purpose of testing at this point is to maintain visibility of the failure.

7.4 SEM FAILURE ISOLATION PROCEDURE

It is important that the SEM examination not influence the circuit failure, so it is pertinent that the beam parameters be selected accordingly. If in doubt use the lowest beam voltage. Use the functional test data to determine at what point in the circuit to begin. The circuit should be examined beginning at the last circuit which is known to be operating correctly. For example if functional testing indicates a defective row decode, this indicates addressing is functioning correctly and the starting point would be the address outputs.

Using a TV or fast scan rate, evaluate the input and output responses for each functional block. It is helpful to compare a known good circuit's operation with the circuit being evaluated. For example, if a decode circuit is being evaluated select an address scheme which alternately addresses the decode circuit on either side of the suspect circuit. The bit map will quickly show which address codes are required. Continue evaluating each functional block until the failure is isolated.

Once the failure is isolated to a specific block then this block is examined to locate the area of the failure. This is best accomplished by documenting the failed circuit on a voltage contrast photograph. The area of the failure is located using the photograph. The characterization photograph can be used for comparison. When the failure is isolated use the least degrading techniques first in attempting to identify the cause; i.e., light microscope, mechanical probe, SEM EBIC etc.

One point to consider, the quality of an isolation is judged by the effect the isolation technique has on the failure. If experience or failure symptoms suggest the SEM may be unsatisfactory for isolating the failure, then it should not be utilized. Every technique has its limitations and the analyst must make this judgment.

7.5 SUMMARY

SEM isolation is a qualitative tool. It provides rapid isolation with minimal damage and good success. Quantitative evaluation is obtained by mechan-

ical probing and measurement.

8.0 LIMITATIONS OF SEM EVALUATION METHODS

As stated earlier there were no observed occurrences where the electron beam influenced the circuit operation. Such interference could occur at higher beam voltages and currents than were used for voltage contrast imaging in this study. The limitations that are described here are primarily based upon the experience realized during this study.

8.1 BIPOLAR AND METAL GATE MOS

8.1.1 VOLTAGE CONTRAST

8.1.1.1 Beam Voltage/Current

The voltage contrast sensitivity is a function of residual charge on the subject surface. This charge accumulation is a function of the beam voltage and current. Bipolar and metal gate MOS can generally tolerate higher voltages. Therefore the limitation of beam voltage is determined by the point where voltage contrast is adversely affected. There are two preferred beam voltage operating points. One is where minimal electron penetration and charge accumulation is realized. This operating point is based on the relationship of incident electrons versus reflected electrons. During this study a beam voltage of 1 KV was used for this operating point. The second operating point is where the primary electrons begin to penetrate the surface oxide. This increases the conductivity of the oxide and reduces the surface charge accumulation. As the beam voltage is further increased this advantage is diminshed until voltage contrast is lost completely. This operating point was typically in the area of 5 KV during this study and has been found to be 8 to 10 KV on circuits which have the original passivation in place. The beam current should be set to as low a level as practical. There are two factors to consider in determining the proper beam current level. They are image signal to noise and image voltage contrast sensitivity. The beam current should be adjusted to provide a reasonable image signal to noise ratio. Once this point is reached the beam voltage and current are adjusted to optimize the voltage contrast sensitivity.

8.1.1.2 Low Signal Circuits

The standard SEM secondary electron detection systems generally do not provide sufficient sensitivity to detect low level circuit voltage changes. Therefore it was not practical to perform voltage contrast imaging for circuits which contain low level signals. The minimum detectable voltage is in the region of 0.5 to 0.7 volts. The circuits which typically contain these low level signal nodes are sense amplifiers and the majority of I^2L circuitry. Another problem presented by I^2L circuits is the large utilization of buried layer conductors. The low level signals in I^2L circuits has established the need for improved detection systems.

8.1.2 BEAM INFLUENCE

8.1.2.1 Irradiation Degradation

Beam irradiation damage generally occurs whenever the electron range is sufficient to penetrate the surface oxide. The majority of damage occurs in the first 15 - 20 seconds of beam exposure. The amount of damage can typically degrade transistor beta by 50 to 75%. This degradation does not usually affect functional circuit operation but could be misleading and confusing for circuit failure analysis.

8.1.2.2 Beam Voltage/Current

There were no instances of the electron beam influencing circuit operation during this study. Whenever the primary electrons have sufficient range to penetrate the surface oxide, the beam may influence circuit operation. To do so the beam must induce a current into the circuit which produces a change in operation. The induced currents generated by carrier multiplication in semiconductors can be three orders of magnitude above the focused beam current. These current levels are easily capable of disrupting circuit operation in current LSI and VLSI bipolar technology. As the circuit densities increase and circuit node current decreases, the circuit sensitivity to beam induced currents will increase. The best method to avoid beam influence on circuits is to be familiar with acceleration voltage/electron range and potential EBIC generation levels in semiconductors and based upon these data, utilize beam parameters which are well below the point of influencing circuit operation.

8.2 SILICON GATE NMOS

8.2.1 VOLTAGE CONTRAST

8.2.1.1 Beam Voltage/Current

The beam voltage limitation is dictated by irradiation degradation. The beam current for silicon gate NMOS was limited to a maximum of 50 pA. Utilizing beam currents above 50 pA resulted in reduced voltage contrast sensitivity. All voltage contrast evaluation of silicon gate NMOS was performed at beam voltages of 1.0 to 1.3 KV.

8.2.1.2 Low Signal Circuits

In MOS technology, circuit operation is controlled by voltage level as opposed to bipolar circuitry which is controlled by current level. Therefore MOS circuitry is more compatible with voltage contrast imaging. No low signal voltages were encountered for MOS circuits which presented a limitation to voltage contrast imaging. The MOS circuits were found to be less tolerant to passivation etching. This resulted in greater passivation thickness on these circuits for voltage contrast evaluation, which reduced the subsurface voltage contrast sensitivity. The MOS circuits presented more problems from high field changes which produced significant image shifting during operational imaging. This problem was confined to the circuits requiring 12 v supply voltage.

8.2.2 BEAM INFLUENCE

8.2.2.1 Irradiation Damage

The silicon gate NMOS circuits showed a high susceptibility to irradiation damage. This required that these circuits be examined with electron beam voltages of less thant 1.5 KV. When beam voltages reached 3 to 5 KV circuit degradation began to occur. On the 16 K bit EPROM the first indication was an erasure of the programmed data. The first indication on the RAM circuits was functional failure. Also it was determined if the beam voltage was increased to 8 KV the resultant circuit damage could not be reversed through high temperature annealing. It was not determined what damage had occurred as a result of the 8 KV beam exposure. Irradiation damage occurred on the 4096 bit dynamic NMOS RAM at a beam voltage of 1.3 KV. This was determined to have resulted from removing too much glass passivation. The silicon gate NMOS circuits would not tolerate electron penetration into the gate oxide.

8.2.2.2 Beam Voltage/Current

There were no instances where the electron beam influenced circuit operation. These circuits will not tolerate electron penetration of the surface oxide which is necessary to realize carrier multiplication. The absorbed current levels were not sufficient to affect circuit operation. This may become a limiting factor as circuit densities increase and circuit node currents are reduced.

9.0 CONCLUSIONS

SEM applications were shown to provide a significant improvement in both device characterization and failure isolation. These applications are complementary to light microscopy observations, and on a combined basis provide a significant improvement in developing circuit schematics. The implementation of the SEM applications does not require an extraordinary instrument capability.

Functional mapping was demonstrated to be practical for accurately portraying circuit operation for static and dynamic memory circuits. Functional mapping provides operating circuit signals superimposed on a secondary electron image. This allows complete operational circuit interpretation from the voltage contrast micrograph. The isolation of circuit failures has been significantly improved through the application of functional mapping. Circuit failures can be quickly isolated and extensive mechanical probing has been eliminated.

EBIC was shown to provide useful data for bipolar circuits in general and is a necessary requirement for identifying buried layer interconnections in I^2L circuits. EBIC can provide identification of diffusion polarity for a major portion of a circuit. EBIC is also a valuable method for locating diffusion faults and junction overstress sites. These applications were not demonstrated during this study because it was not practical to generate these failure mechanisms.

These SEM applications were described in detail and procedures were developed to aid in their utilization. These data include SEM instrument operating guidelines, functional circuit testing, device characterization and failure isolation procedures, and detailed device characterization results. This study was successful in developing the necessary procedures and demonstrating their practicality in characterization and failure isolation for complex memory devices. Their true test will come with the evaluation of additional circuit types and utilization in the isolation of actual circuit failures.

10.0 RECOMMENDATIONS

The results of this study justify the evaluation of other complex circuit families to determine the feasibility for using similar applications for circuit characterization. One area which presents a significant problem to the failure analyst is the microprocessor family.

It is apparent that quantitative voltage and time measurements utilizing the electron beam are currently needed to support complex circuit failure analysis. Increased voltage sensitivity is currently needed for the characterization and failure isolation of I^2L technology. The physical damage and circuit loading introduced by mechanical probing presents a serious problem for complex circuit analysis. This problem will become more serious as the circuit complexities increase. Electron beam probing currently requires 25 to 50 pA of beam current. This may provide an order of magnitude of margin over present day complex circuit node currents. Further improvement of present applications or development of new applications will be required for characterization and failure isolation of next generation circuit technologies. The confidence factor for safe removal of glass passivation without adverse effects on the circuit failure, dictates prior evaluation of like devices from a common lot. This is an area of needed improvement which is common to all failure isolation techniques.

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